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DESIGN, ANALYSIS, AND PROTOTYPE FOR ONE-CYCLE CONTROLLER

by

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December 1996

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As the Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of DC electrical distribution systems rather than traditional AC distribution systems. The DC Zonal Electrical Distribution System is a prime candidate for direct application to modern power distribution. This system employs solid-state conversion devices to supply ships loads from one of two high-voltage DC busses. A new type of control technique known as One-Cycle Control has recently been proposed which may be of use in the control of these power converters. Specific advantages of this technique include no steady-state nor dynamic error between the control signal and the controlled variable, robust performance, power source perturbation rejection, fast dynamic response to changes in the control signal, general switching applications, and automatic switching error correction. The focus of this thesis is to validate the One-Cycle Control theory through simulation and testing of a prototype controller.

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DESIGN, ANALYSIS, AND PROTOTYPE FOR ONE-CYCLE CONTROLLER

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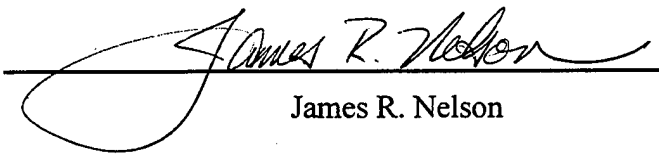
Author: 

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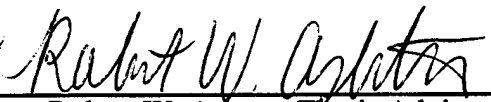
Approved by: 

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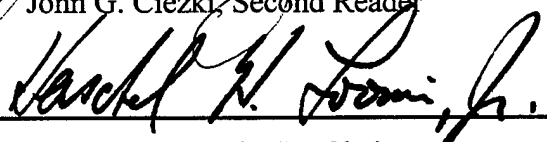

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ABSTRACT

As the Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of DC electrical distribution systems rather than traditional AC distribution systems. The DC Zonal Electrical Distribution System is a prime candidate for direct application to modern power distribution. This system employs solid-state conversion devices to supply ships loads from one of two high-voltage DC busses. A new type of control technique known as One-Cycle Control has recently been proposed which may be of use in the control of these power converters. Specific advantages of this technique include no steady-state or dynamic error between the control signal and the controlled variable, robust performance, power source perturbation rejection, fast dynamic response to changes in the control signal, general switching applications, and automatic switching error correction. The focus of this thesis is to validate the One-Cycle Control theory through simulation and testing of a prototype controller.

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I. INTRODUCTION

A. RESEARCH FOCUS

The purpose of this thesis research is to establish the feasibility of the One-Cycle Control technique [1] within the scope of the future Naval power distribution systems. The One-Cycle Control technique was first proposed in 1991 as a new large-signal nonlinear control technique which can control the duty cycle of a switch such that the average value of the switched variable in each period is precisely proportional to the control reference. The specific advantages include no steady-state error nor dynamic error between the control signal and the controlled variable, robust performance, power source perturbation rejection, fast dynamic response to changes in the control signal, general switching applications, and automatic switching error correction. The results of this research will be a stepping stone towards future applications of this control technique.

As the Navy searches for new and better ways to improve the performance, reliability, and simplicity of modern warships, basic research into concepts facilitating this goal must be undertaken. In the arena of power distribution systems, a future design has been suggested by Dade [7] in which the primary power transmission lines of the vessel would carry DC power at fairly high voltage levels. The power from these busses would be distributed throughout the vessel through the use of solid-state power conversion devices. The devices must be able to convert the distributed DC voltage level to the DC or AC voltage levels of the loads. A modular control system which is able to

perform these functions reliably and simply would be of great benefit to future ship power system designers. One-Cycle Control is a viable candidate for utilization in these future power systems due to the inherent simplicity of the technique and the possibility of modular design. This research will illuminate the key features of One-Cycle Control.

The areas explored include a theoretical development of One-Cycle Control, simulations of a basic One-Cycle controller, and a practical implementation of a prototype One-Cycle controller with a direct current power conversion device known as a buck chopper. This chapter further specifies the concepts of future power systems and the place One-Cycle Control may hold within this endeavor. Chapter II describes the test platform for the One-Cycle controller prototype. Chapter III presents the theoretical basis for One-Cycle Control. Chapter IV presents the simulation results of the basic controller, open-loop control of the buck chopper and closed-loop control of the buck chopper. Chapter V presents the prototype controller topology and performance characteristics of the basic controller, open-loop control, and closed-loop control bench tests. Chapter VI presents the conclusions of this research and recommended future studies.

B. DC ZONAL ELECTRICAL DISTRIBUTION SYSTEM

One particularly interesting shipboard electrical distribution system, advocated and described by Doerry [6], is the DC Zonal Electrical Distribution System (DC ZEDS). This system promotes modularity of design within vessels by specifying that there be only main power generation equipment, a port and starboard main power DC bus and all other electrical distribution achieved through the use of DC zones. Figure (1-1) shows

the basic topology of a zone within the DC ZEDS architecture. The port and starboard DC busses for each zone carry 1000 V DC power throughout the ship with higher voltages possible as semiconductor switch capabilities improve. A Ship Service Converter Module (SSCM) receives the 1000V DC input and produces a regulated power at a lower DC voltage for use in Ship Service Inverter Modules (SSIM) and intermediate voltage DC loads. The SSIM takes the lower DC voltage from the SSCM and converts it into regulated AC power for use in the ships AC loads. Vital loads would utilize both main power busses through diode steering.

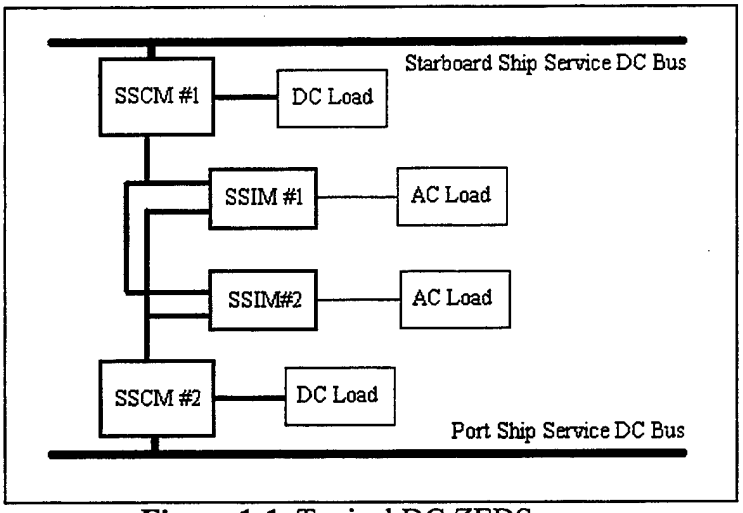

Figure 1-1, Typical DC ZEDS zone

The types of SSCM's would be high voltage to intermediate voltage as seen in the figure and intermediate to lower voltage for power supplies for those ships DC loads which require an even lower voltage. The AC outputs of the SSIM's would be at various voltage levels and frequencies in order to supply all different types of AC loads.

Some advantages of utilizing a zonal DC power distribution system with dispersed solid-state power converters are cost savings associated with the elimination of large electromechanical switchgear, optimization of the power generation equipment to provide only the main DC power busses, minimization of power conversion steps between generator and end user, and the potential advantage of fast semiconductor devices improving shipboard power management under normal and casualty conditions. Also of great interest is the commonality and modularity of the major building blocks within the DC ZEDS concept. The Navy could save appreciably in the reduced training and manning requirements as the electrical power distributions systems across the classes of ships become more common. In addition, as future technologies come to fruition, the best power conversion modules available can be easily implemented into the system by ensuring interface criteria are met.

One such technology discussed by Doerry is the Power Electronic Building Block [6].

> The Power Electronic Building Block (PEBB) is a new device that integrates within a single unit, all the elements required for generalized power processing. It will replace many single application multi-component power control circuits with a single device that delivers digitally synthesized power under device level control. PEBBs are a standard set of snap together parts that start at the semiconductor chip level and build up to the system level while integrating intelligence at various levels for custom performance - a power electronic analogy of a microprocessor.

Clearly this is an exciting possibility for the future of power electronics; however, copious amounts of basic research must be accomplished before such a device can be realized.

For now, the SSCM and SSIM must take on the roles as the major power conversion devices within the DC ZEDS architecture. The SSCM must necessarily be a DC step-down converter. One of the most popular topologies for this conversion process is the buck chopper, to which One-Cycle Control is well suited. The SSIM could be one of many inverter topologies; however, the basic control needs for these topologies might be fulfilled by One-Cycle Control. The One-Cycle Control technique must be extendible to any type of switching control scenario encountered by the types of converters described.

The test bed developed for the One-Cycle controller incorporates a buck chopper. This will allow for testing the capabilities of the technique in an application which is fundamental to the DC ZEDS architecture. A basic derivation of the governing equations for a buck chopper is presented in the next chapter, along with a description of the physical test bed built for the prototype controller.

II. THE POWER SECTION

A. GENERAL DESCRIPTION

The buck chopper, or step-down converter, is a DC-to-DC converter in which the input voltage is switched in a manner to produce an output voltage which is less than the input voltage. The circuit incorporates a semiconductor switch, an output filter to reduce the ripple, and a free-wheeling diode to ensure that the inductor current has a path for flow when the switch is open.

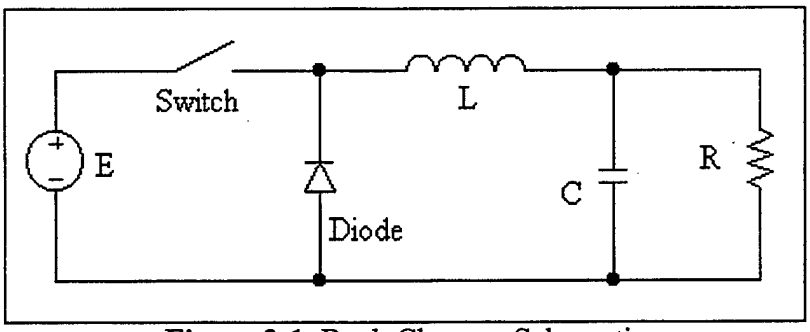

Figure 2-1, Buck Chopper Schematic

1. Basic Buck Chopper Topology

The topology for the buck chopper is shown in Figure (2-1). There are two normal modes of operation for the buck chopper depending on the current through the inductor. The primary mode of operation is characterized by the current through the inductor being continuous. In the other mode of operation the current through the inductor will reach zero and remain so until the power source supplies more power to the circuit. This thesis will only address the continuous inductor current mode of operation due to its linear input-to-output characteristic. A description of the discontinuous inductor

current operation of the circuit may be seen in reference [3]. The switch and diode in the buck chopper circuit are assumed to be ideal for the derivations which follow.

Referring to Figure (2-1), the DC power source voltage is E and the switch is operated at a constant frequency. When the switch is 'on', the diode is reverse biased and the inductor accumulates energy from the source. When the switch 'opens', the source is removed from the circuit and the free-wheeling diode provides a path for the inductor current which supplies its stored energy to the capacitor and the load. The ratio of the 'on-time' to the switching period is termed the duty cycle. The capacitor reduces the output ripple to an acceptable value, determined by the sensitivity of the load. In most cases, the AC ripple is much smaller than the DC output voltage, with a reasonable value being 0.5 % or less. The net result is that the LC low pass filter passes the average of the switched voltage while eliminating the high-frequency switching noise. For notation purposes, capital letters will denote average values while lowercase letters will denote instantaneous quantities. During the time that the switch is closed, the governing equations are:

$$E = v_L(t) + v_C(t) \tag{2-1}$$

$$E = L\frac{di_L(t)}{dt} + V_C \tag{2-2}$$

$$\frac{di_L(t)}{dt} = \frac{E - V_C}{L} \tag{2-3}$$

$$di_L(t) = \frac{E - V_C}{L} \cdot dt \tag{2-4}$$

$$I_{max} - I_{min} = \frac{E - V_C}{L} \cdot DT \tag{2-5}$$

where the value of the output capacitance is assumed to be large enough so that v_C is equal to V_C, the duty cycle of the switch is D, and the period of the switch is T. The assumption that the capacitor voltage is a DC value can be seen from:

$$v_C(t) = \tilde{v}_C(t) + V_C \tag{2-6}$$

where $\tilde{v}_C(t)$ is the capacitor AC ripple voltage and $\tilde{v}_C(t) << V_C$.

During the time that the switch is 'open', the equations which govern the circuit operation are:

$$0 = v_L - V_C \tag{2-7}$$

$$0 = L\frac{di_L}{dt} + V_C \tag{2-8}$$

$$\frac{di_L}{dt} = \frac{-V_C}{L} \tag{2-9}$$

$$di_L = \frac{-V_C}{L} \cdot dt \tag{2-10}$$

$$I_{min} - I_{max} = \frac{-V_C}{L} \cdot (1 - D) \cdot T \tag{2-11}$$

By equating Equations (2-5) and (2-11), the expression for the input-to-output voltages can be found:

$$V_C = D \cdot E \tag{2-12}$$

Typical waveforms for the buck chopper are shown in Figure (2-2). From the beginning of a period T until the time shown as DT, the switch is 'shut' and the current through the

inductor i_L rises. The current through the switch i_s is identical to the inductor current while the switch is 'shut' so it also rises during this time interval. The diode is reverse biased so the diode current i_D is zero during this interval. The source voltage is connected to the input side of the inductor while the capacitor is connected to the output side of the inductor, so the inductor voltage v_L is seen as the difference between the two for this interval. When the switch 'opens', the source is isolated from the rest of the circuit and the free-wheeling diode allows for current to flow as described previously.

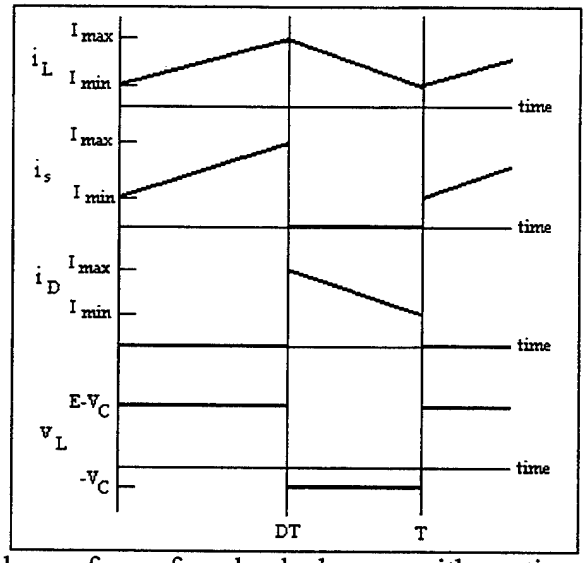

Figure 2-2, Typical waveforms for a buck chopper with continuous inductor current

During this interval the inductor current falls while the switch current is zero due to the switch being 'open'. The diode current is identical to the inductor current during this interval. Finally, by applying Kirchoff's voltage law to the loop which includes the inductor, diode and capacitor, and assuming zero voltage drop across the diode, the

inductor voltage is seen to be equal to the opposite of the capacitor voltage. These waveforms should be referred to during the following discussion.

In order to select the an inductor for the circuit which will prevent the discontinuous current mode from occurring, the average inductor current is found:

$$I_L = \frac{I_{max} - I_{min}}{2} \tag{2-13}$$

and the average load current is found:

$$I_R = \frac{V_C}{R} = I_L \tag{2-14}$$

where the inductor current is assumed to be equal to the load current due to the large capacitor size. By equating Equations (2-13) and (2-14), the maximum inductor current is found:

$$\frac{I_{max} + I_{min}}{2} = \frac{V_C}{R} \tag{2-15}$$

$$I_{max} = \frac{2V_C}{R} - I_{min} \tag{2-16}$$

Substituting Equation (2-16) into Equation(2-11) yields:

$$I_{min} - \frac{2V_C}{R} + I_{min} = \frac{-V_C}{L} \cdot (1-D) \cdot T \tag{2-17}$$

$$2I_{min} = \frac{-V_C}{L} \cdot (1-D) \cdot T + \frac{2V_C}{R} \tag{2-18}$$

By setting the minimum inductor current to zero, the value of the critical inductance is found:

$$L_{crit} = \frac{T \cdot R}{2} \cdot (1-D) \tag{2-19}$$

This minimum inductance value must be satisfied in order to ensure continuous current operation of the buck chopper.

2. Component Selection

For laboratory implementation the nominal duty cycle was selected to be 0.693 based on an input voltage of 300 V_{DC} and an output voltage of 208 V_{DC} using Equation (2-12). The operating frequency for the switch was selected as 20,000 Hz in order to reduce the audio output of the circuit and to allow for a reduction in the required output filter component sizes. The resulting period of the switch is 50 μsec. A load resistance of 150 Ω was selected in order to define the minimum load current expected, yielding a critical inductance, from Equation (2-19), of 1.15 mH. The components utilized in constructing the circuit are summarized in Table (2-1).

Switch	International Rectifier IRGT1090U06 Insulated Gate Bipolar-Junction Transistor (IGBT), with antiparallel diode
Capacitor	Sprague Powerlytic 2000 μF, 450 V_{DC}
Inductor	1.35 mH, hand wound

Table 2-1, Circuit components

The combined switch and diode pack used in the Buck Chopper is a high speed (25 to 100 kHz) and high power (600 V, 90 A) device. As such, the voltage drops across these components for switching transients and in the steady state are small (about 2 V) compared to the voltages and currents being switched, thus justifying the assumption that the voltage drops across these components are zero for the equations derived in this chapter.

B. IGBT DRIVER CIRCUIT

The main switch used in the construction of the power section requires a set of input voltages on the gate terminal which are properly controlled in magnitude with a relatively high value of source and sink currents in order to operate properly. The circuit constructed for use with the IGBT is shown in Figure (2-3).

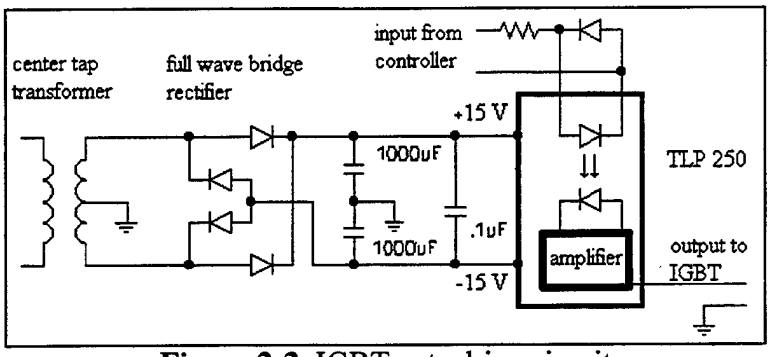

Figure 2-3, IGBT gate drive circuit

The heart of the driver circuit is the TOSHIBA TLP 250 gate drive photo IC coupler. This device combines the high speed, high gate current, and optical isolation of the control circuit in one package for ease of use. The 120/14 V_{AC}, center-tap transformer, diode configuration, and 1000 μF capacitors produce an unregulated 10 V and -10 V DC power supply which has a floating ground. The 0.1 μF capacitor reduces any high-frequency noise seen on the power supplies as a result of switching transients on the TLP 250. The high-speed diode and resistor connected to the TLP 250 diode allow for proper currents to be sent to the TLP 250 diode in order to avoid damage to the chip. The zener diodes prevent the voltage on the IGBT gate from becoming too large thus protecting the

gate circuit from damage. Finally, the output resistor ensures proper impedance matching of the IGBT gate and driver circuit.

The operation of the circuit is straightforward. A 15 V input to the driver circuit will cause the LED on the TLP 250 chip to assume the 'on' state. The optical sensor within the chip will detect the condition of the diode and cause the output amplifier on the chip to set the voltage on the IGBT gate 'high', thus turning it on. The stray capacitance, associated with the IGBT gate circuit and leads between the IGBT and driver circuit, is rapidly charged due to the high source current capability of the TLP 250 output amplifier.

When the input voltage to the driver circuit is set to -15 V, the TLP 250 diode is turned off, and the output amplifier will set the gate voltage negative. Once again, the current sinking ability of the output amplifier enables the charge on the IGBT gate to be removed very rapidly, enhancing the ability of the driver to be used in higher speed circuit applications.

C. POWER SECTION TEST RESULTS

The power section was tested at frequencies from 5 kHz to 40 kHz and power levels from 10% to 167% rated power (3 kW). The switching and diode loss from the IGBT pack was less than 60 W at the highest power levels tested, as measured from the input and output voltage and current values. Circuit stability for all conditions tested was verified and the inductor current was found to be continuous at minimum load. Operation of the driver circuit was acceptable for all frequencies tested, with the input voltages

ranging from 5 to 15 V and -5 to -15 V. The audio output at frequencies below 20 kHz was substantial, justifying the choice for the switching frequency of the controller to be at or above 20 kHz.

With the test bed built and tested, the stage is set to present the theory behind One-Cycle Control. Chapter III describes the fundamentals and advantages of this control scheme.

III. ONE-CYCLE CONTROL

A. BASIS FOR OPERATION

According to Smedley and Cuk [1], there is a need for a large-signal nonlinear scheme to control switching converters, which are best described as pulsed nonlinear dynamic systems. A pulsed, nonlinear control scheme, if properly implemented, should yield faster dynamic response, reject power source perturbations better, and be more robust than a linear, feedback-based control scheme. The reason for this is that the control scheme will better match the nature of the system it is controlling. One-Cycle Control, the proposed method of nonlinear control, may exhibit these advantages as well as zero steady-state and dynamic error between the control signal and the controlled variable.

1. Theory of Operation

From Smedley and Cuk [1],

...a switch operates according to the switch function k(t) at a frequency $f_s=1/T_s$,

$$k(t)=\begin{cases}1 & 0<t<T_{ON}\\ 0 & T_{ON}<t<T_s.\end{cases} \tag{3-1}$$

In each cycle, the switch is on for a time duration T_{ON} and is off for a time duration T_{OFF}, where $T_{ON}+T_{OFF}=T_s$. The duty-ratio $d=T_{ON}/T_s$ is modulated by an analog control signal $v_{ref}(t)$. The switch input signal x(t) is chopped by the switch. The frequency and pulse width of the switch output y(t) is the same as that of the switch function k(t), while the envelope of y(t) is x(t)...

$$y(t)=k(t)\cdot x(t) \tag{3-2}$$

...Suppose the switch frequency f_s is much higher than the frequency bandwidth of either the input signal x(t) or the control signal $v_{ref}(t)$; then the effective signal carried in the switch output is

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)\cdot dt \tag{3-3}$$

$$\approx x(t)\cdot\frac{1}{T_s}\int_0^{T_{ON}} dt \tag{3-4}$$

$$= x(t)\cdot d(t) \tag{3-5}$$

$$= x(t)\cdot v_{ref}(t). \tag{3-6}$$

The output signal y(t) of the switch is the product of the input signal x(t) and the control signal $v_{ref}(t)$; therefore, the switch is nonlinear. If the control signal $v_{ref}(t)$ is constant, for example $v_{ref}(t)=D$, the output signal of the switch is Dx(t), which is the case when the switch is used for digital signal processing. In power processing applications, for example a power amplifier, the input x(t) usually represents the power, while the control signal $v_{ref}(t)$ represents the signal to be amplified. In the ideal case the input power x(t) is constant X; therefore, the output signal $y(t)=Xv_{ref}(t)$. However, in reality perturbations always exist in the input power x(t); hence, the output signal y(t) contains the power disturbance as well.

If the duty-ratio of the switch is modulated such that the integration of the chopped waveform at the switch output is exactly equal to the integration of the control signal in each cycle, i.e.

$$\int_0^{T_{ON}} x(t)\cdot dt = \int_0^{Ts} v_{ref}(t)\cdot dt \tag{3-7}$$

then the average value of the chopped waveform at the switch output is exactly equal to the average value of the control signal in each cycle, i.e.

$$\frac{1}{T_s}\int_0^{T_{ON}} x(t)\cdot dt = \frac{1}{T_s}\int_0^{Ts} v_{ref}(t)\cdot dt \tag{3-8}$$

Therefore, the output signal is instantaneously controlled within one cycle, i.e.

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)\cdot dt = \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)\cdot dt = v_{ref}(t) \tag{3-9}$$

The technique to control switches according to this concept is defined as the One-Cycle Control technique. With One-Cycle Control, the effective output signal of the switch is

$$y(t) = v_{ref}(t) \tag{3-10}$$

The switch fully rejects the input signal and linearly all-passes the control signal v_{ref}; therefore, the One-Cycle Control technique turns a non-linear switch into a linear switch.

Equation (3-19) may be further justified to the reader by stating that the 'frequency' of the time-varying reference voltage must be significantly smaller than the switching frequency such that in one period the reference voltage can be modeled as a constant. With this assumption, the integral of the 'constant' reference voltage evaluated over the times specified will equal the 'constant' reference voltage.

The schematic diagram for a One-Cycle controlled buck chopper is shown in Figure (3-1). The switched variable for this converter is the diode voltage, v_D. The output voltage of the buck chopper is the average value of the diode voltage [1]:

$$V_R = \frac{1}{T}\int_0^T v_D(t)\cdot dt = \frac{1}{T}\int_0^{T_{ON}} e\cdot dt = k\cdot v_{ref} \qquad (3\text{-}11)$$

where k is the gain for the control system compared to the power system. The scaled reference voltage signal matches the output voltage during each period, hence, One-Cycle Control is achieved. The linear transfer function of the system is:

$$\frac{v_R(s)}{v_{ref}(s)} = \frac{1}{LCs^2 + \frac{L}{R}s + 1}. \qquad (3\text{-}12)$$

For the circuit in Figure (3-1), the clock signal begins the operation of a new period. A clock pulse will turn on the main switch and ensure that the integrator is enabled. The main switch will conduct current and deliver power to the load as well as recharge the capacitor.

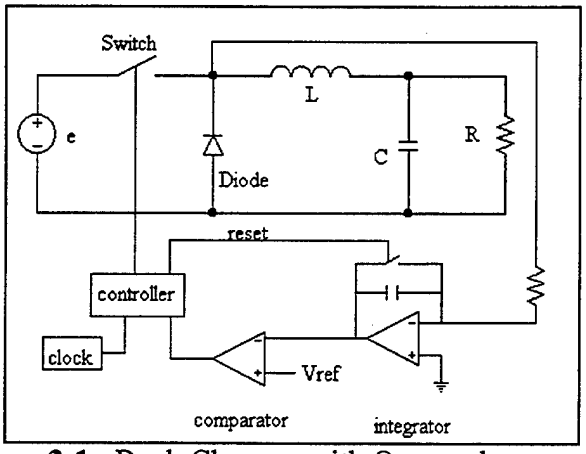

Figure 3-1, Buck Chopper with One-cycle controller

Meanwhile, the integrator will begin integration of the input voltage signal, scaled to controller voltage levels. The integrator output is continuously compared to the reference voltage, and when they become equal, the comparator will change states. This action causes the controller to reset the integrator to zero and turn off the main switch simultaneously. For the remainder of the period, the free-wheeling diode in conjunction with the inductor and capacitor deliver energy to the load. The magnitude of the input voltage is directly proportional to the slope of the integration. A higher input voltage will result in a steeper integration slope, hence a shorter on-time for the main switch.

B. POWER SOURCE PERTURBATION REJECTION

A major shortcoming in feedback control systems as opposed to One-Cycle Control is revealed when the input power source has a perturbation. The perturbation must be felt at the output of the system before the feedback loop can correct for it. With One-cycle Control, the input perturbation will immediately cause a change in the slope of the integration for the period. This feedforward action causes the power source

perturbation to change the duty cycle on a per period basis. It would be beneficial if the buck chopper were not affected by source voltage perturbations.

Figure (3-2) shows the theoretical duty cycle adjustment to a step change in the input voltage. Note that the duty cycle is defined by the amount of time per period that the trace labeled Duty Cycle is in the 'high' state. For the two cases where the source voltage is constant throughout a number of cycles, a steady-state value of the duty cycle is attained. When the source voltage rises during a cycle, the integrator immediately senses this change and the slope of the integration voltage rises accordingly. The higher slope results in the Duty Cycle signal toggling to a 'low' state earlier into the period. Note that this period is defined by a dynamically changing duty cycle and that the new steady-state duty cycle is achieved during the next cycle.

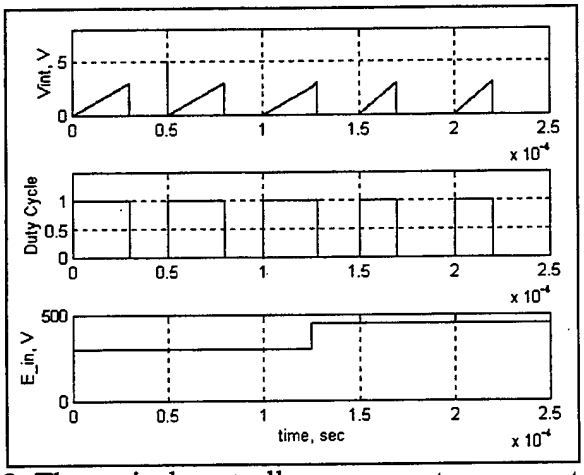

Figure 3.2, Theoretical controller response to source step change

A similar result can be found by allowing the source voltage to decrease, resulting in a less steep integration voltage and larger duty cycle in the steady state.

C. REFERENCE VOLTAGE FOLLOWING

An important feature of this control scheme is the ability of the controller to follow the reference voltage in each period, allowing for the general control of a switch in any converter topology. By allowing the reference voltage to vary in any manner desired, the flexibility of the control method is shown. A possible application of this phenomenon is to use a dynamically changing reference voltage in order to implement feedback loops to eliminate transient or steady-state errors. This method will be explored later.

1. Step Change in Reference Voltage

The ability of the controller to immediately respond to a change in the reference voltage is shown in Figure (3-3). The reference voltage is seen to change in a step-wise fashion and the resultant integration is allowed to continue further into the period in question.

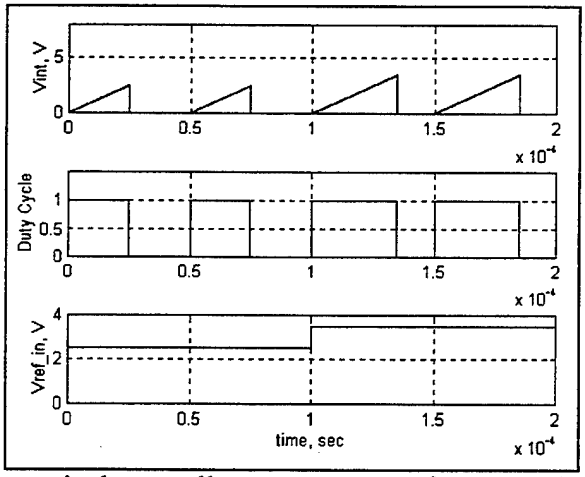

Figure 3-3, Theoretical controller response to reference voltage step change

When the integration voltage equals the reference voltage, the duty cycle for that period is obtained. The new, steady-state duty cycle is seen to be higher, with the time change from one steady-state condition to another contained within one switching period.

Since the output of the converter is not a control variable, a step change in the duty cycle will cause varying degrees of oscillation in the LC output circuit depending on the value of the load. The smaller the load, the greater the oscillations. This effect will be examined further in a later chapter.

2. Sinusoidal Reference Voltage

A powerful result of the instantaneous reference voltage following capability of this control scheme is the ability to generate control signals for AC inverters. A typical method for inverter control is sine-triangle pulse-width modulation, hereafter referred to as sine PWM. In this method, shown in Figure (3-4), a triangle wave at the desired switching frequency and a sine wave at the desired output frequency are fed into a comparator circuit and the resultant set of control pulses is generated.

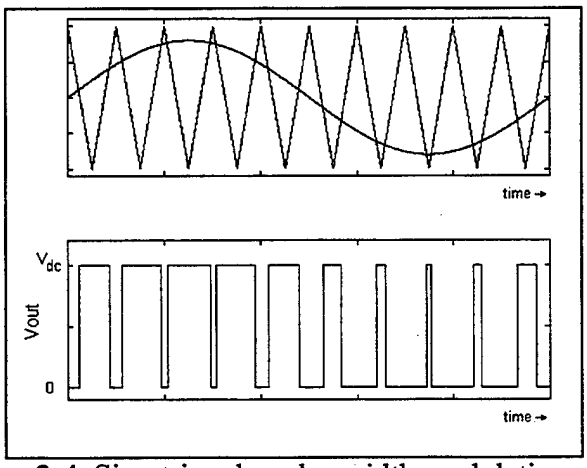

Figure 3-4, Sine-triangle pulse-width modulation signal

These control pulses define the duty cycle signal which is used in a properly constructed inverter to produce the AC power signal desired.

The One-Cycle Controller is able to produce the same set of control pulses as the sine PWM scheme. Figure (3-5) shows the expected output of the controller given a reference voltage input that is sinusoidal.

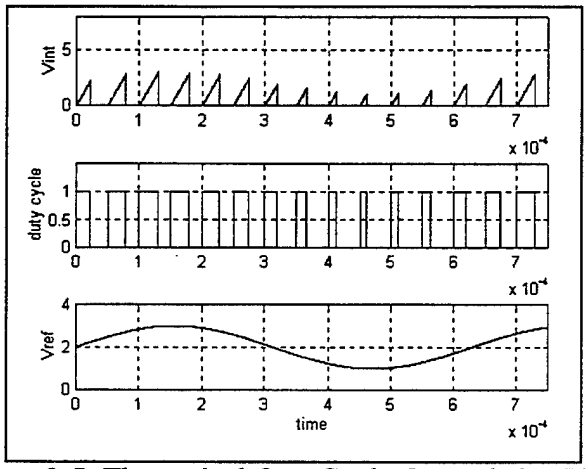

Figure 3-5, Theoretical One-Cycle Control sine PWM

Note that the resultant wave form for the duty cycle is the same as that in Figure (3-4). An added advantage of the One-Cycle Control method for inverter switching is that the source voltage being fed into the inverter does not need to be a tightly controlled DC signal, since the power source perturbations should be rejected as the integration effect of the controller causes the correct amount of power to be delivered in each cycle.

D. SWITCHING ERROR CORRECTION

Perhaps one of the most interesting phenomena with the One-Cycle Control method is the automatic correction of the errors introduced by the non-ideal switch and diode in the power circuit. With the integrator reset time much smaller than the switching period, this automatic error correction is valid. The basic method used to implement this feature of One-Cycle Control is to reset the integrator in a very short period of time concurrent with the opening of the main buck chopper switch. The integrator is then allowed to free run until it is reset in the next cycle by a like event. During the free-run time, any perturbations will be seen by the integrator and their effect will be taken into account by the controller. Note that the sensing location for the controller with automatic error correction necessarily must be the diode voltage.

The effects which are taken into account by the integrator are the on-state voltage drop of the diode, the on-state voltage drop of the switch, and the transients associated with the switch. The integrator is seen to start from a non-zero point at the beginning of the period as a result of the voltages discussed above. When the main switch transitions from an on to off state and vice-versa, a voltage transient will occur. This transient will be detected by the integrator, which is active for all but the very short period of time required to reset the integration voltage to a zero reference, and smoothed in the controller integration for the period in question. The diode will also exhibit transient as well as steady-state voltage drops. Once again, these voltage errors will be smoothed by the use of an integrator in the control scheme. The net result is that the integrator will most likely not start integration from the same potential for each cycle, but rather from a

voltage level which represents the integration of any switch or diode voltage drops or transients. Switching error correction results in the average diode voltage being equivalent to the ordered reference voltage, irrespective of the switching errors introduced.

The effect on the control system when the source voltage rather than the diode voltage is sensed is the elimination of the automatic error correction feature. This may be done in order to simplify the design of the controller or if problems are encountered when sensing the diode voltage. The integrator, however, must be held in the reset state until the start of each cycle to prevent a useless integration of the source voltage.

The next area to be explored is simulation of a One-Cycle controller. The model used is developed in the next chapter and several control scenarios are presented.

IV. COMPUTER SIMULATION

A. OVERVIEW

The simulation environment chosen for modeling the One-Cycle controller was the Advanced Continuous Simulation Language, ACSL (pronounced "axle"). The language is designed for modeling and evaluating the performance of continuous systems described by time-dependent, nonlinear differential equations [9]. The types of simulations performed are on two distinct levels. First, the controller without the buck chopper power section attached, which yielded results on how the controller would respond to various scenarios, and second , the controller with power section, which showed how the overall system would respond. The need for separate types of simulations is two-fold. First, the simulation including the power section takes more time to run (about 20 minutes vs. seconds for the controller only) due to the small step sizes utilized in the computational algorithm and the total time required to be simulated. The step size is required to be small in order to allow for resolution of data within each 50μs period. The simulation without the power section attached was also utilized to generate a control signal suitable for inverter use.

ACSL allows for the user to create a run-time command file in which values for constants, integration step size, communication interval, output variables, and other items which allow for tailoring of each run may be specified. A typical data run would include starting the simulation model and allowing it to run to a specified time, changing various constants to simulate step changes or other variations, and continuing the run to the

specified end time. The state variables are calculated up to the initial run time and are held at their last value until the run continuation is executed or the system is reset. The command file included in Appendix A was utilized for the various simulations performed.

The simulations performed include a source voltage step change, a reference voltage step change, a load resistance step change, a source voltage sinusoidal variation, and a reference voltage sinusoidal variation without the power circuit attached. Other simulations of interest to the designer can easily be implemented by modifying the command file or ACSL code as appropriate.

B. CONTROLLER MODEL

The basic controller model developed for the ACSL environment uses an integration statement which will cause a scaled source voltage to be integrated continuously and divided by the period, as prescribed by the One-Cycle Control technique. The integration value is reset to zero at the end of each cycle, allowing for the next cycle to start from a zero integration level. The value of the integration is continuously compared to the reference value. When the reference value is larger than the integration value, the controller will be simulated as having a high output state. A reference voltage smaller than the integration value will cause a low output state for the controller. The high output state for the controller corresponds to the main buck chopper switch being closed and vice versa. The integration value is allowed to continue

integrating until the period under investigation is completed, since automatic switching error correction will not be investigated.

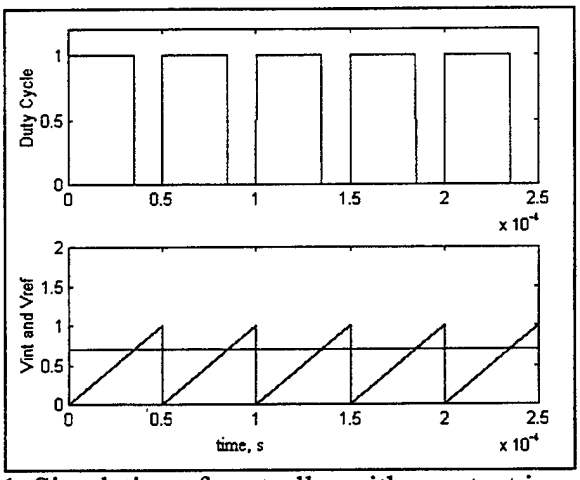

Figure 4-1, Simulation of controller with constant input voltages

The output of the simulated controller is shown in Figure (4-1). The integration value is seen to rise linearly for the constant input voltage applied. When the integration voltage is less than the reference voltage, the duty cycle signal is high and when the integration voltage equals or exceeds the reference voltage, the duty cycle is toggled to the low value. The duty cycle is seen to be a constant steady-state value given the constant reference voltage input. The basic model matches the theoretical result nicely.

1. Step Change in Source Voltage

The ACSL model for the controller given a step change in the source voltage from 300 V to 350 V was simulated. Figure (4-2) shows the results of this simulation.

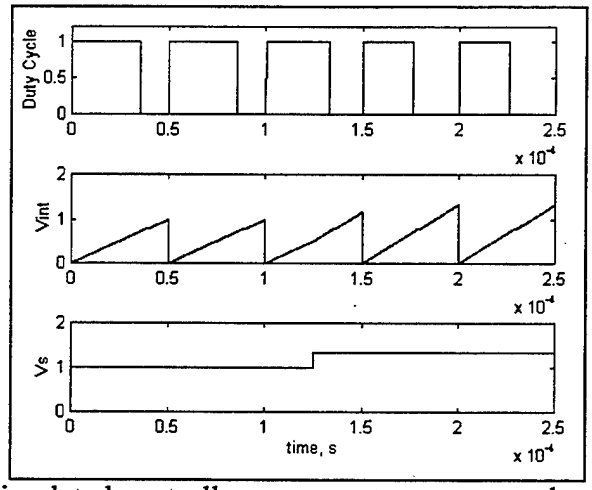

Figure 4-2, Simulated controller response to a source voltage step change

The controller response was identical to the predicted theoretical response. The integrator slope steepened when the input voltage rose, with the resulting duty cycle becoming smaller. Also, the duty cycle change was achieved during one cycle of the integrator, which should yield zero dynamic and steady-state error.

The duty cycle before and after the transient is proportional to the input voltage before and after the transient, with a net result that the output voltage of the controlled circuit should not vary, since the duty cycle was shown to be dynamically adjusted based on the instantaneous source voltage. The basis for One-Cycle Control is illustrated by this simulation result.

2. Source Voltage Sinusoidal Variation

Another interesting application of One-Cycle Control is the rejection of a periodic perturbation to the source voltage. These perturbations in source voltage may be the result of poor filtering in the DC supply to the converter or in the actual DC-to-DC

converter 'front-end'. For instance, if the source to the buck chopper was a pulsed rectifier, a poor filtering network could easily introduce a periodic variation into the supply voltage. One-Cycle Control should eliminate this ripple, given that the frequency of the ripple is well below the switching frequency of the buck chopper. An application of this might also include the elimination of the input filter for the buck chopper altogether.

For the purpose of demonstrating the above principle, the results of simulating a 3.6 kHz, 50 V sinusoidal perturbation riding on a source voltage of 300 V, where the switching frequency is 20 kHz, are shown in Figure (4-3).

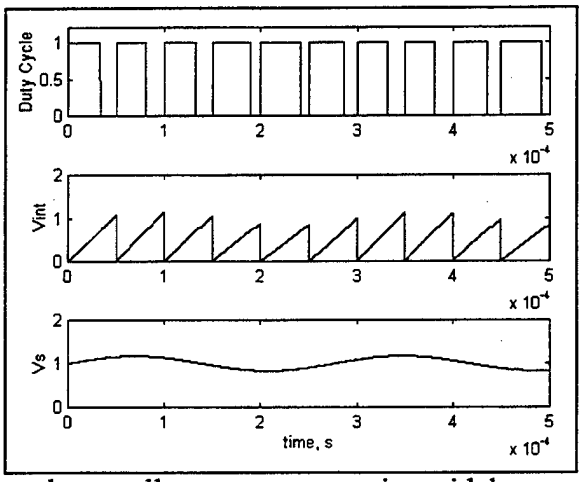

Figure 4-3, Simulated controller response to a sinusoidal source voltage variation

The duty cycle is seen to adjust on a per-period basis in order to pass the same amount of power to the inductor as was passed in the previous cycle. Actual ripple values would typically be on the order of 360 Hz, resulting in a finer control variation on a per-cycle basis.

3. Reference Voltage Step Change

Recall that the expected response to a step change in the reference voltage is a change in the duty cycle from the old steady-state value to the new steady-state value within one cycle. Note that the controller simulation is normalized such that the reference voltage value specified will be equivalent to the ordered duty cycle, e.g. a reference voltage of 0.7 V corresponds to a duty cycle of 0.7. The result of a step change from a reference voltage of 0.7 to 0.8 is illustrated in Figure (4-4). The results of this simulation clearly show that the new steady-state duty cycle is achieved within one period as predicted by theory.

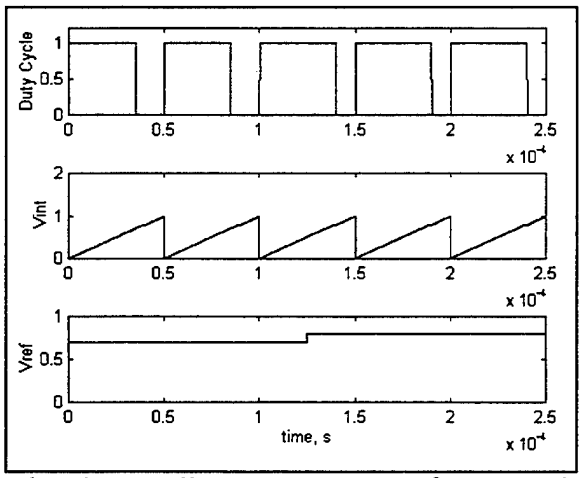

Figure 4-4, Simulated controller response to a reference voltage step change

4. Reference Voltage Sinusoidal Variation

One-Cycle Control can be extended to control any general switched variable. Of particular interest is the ability to generate a control signal which could be used in the implementation of an inverter. Recall that the basic duty cycle sequence of a sine PWM controller is appropriate for the generation of AC power with a properly constructed

inverter. The reference voltage signal applied to the model for the controller was simulated as a sinusoid centered at 0.5 V with a peak to peak amplitude of 0.9 V and a frequency of 3.6 kHz, to obtain a useful time scale. The simulation results for this run are shown in Figure (4-5).

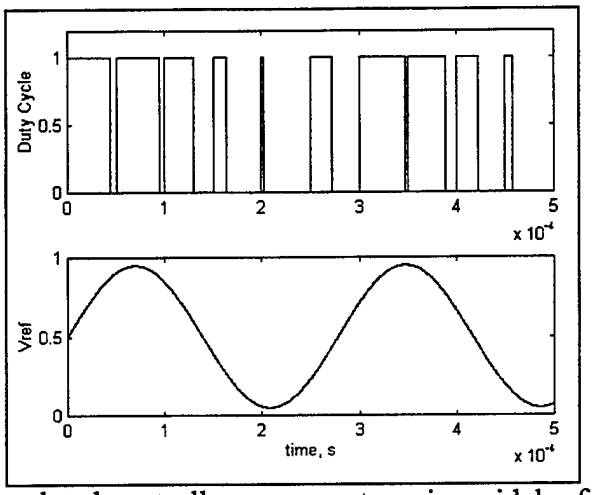

Figure 4-5, Simulated controller response to a sinusoidal reference voltage

The duty cycle variation is identical to that observed in the sine PWM method. The One-Cycle controller is thus shown to be useful not only for DC power generation, but also for the generation of AC power. In the event that three-phase AC power is desired, the method could be extended to that arena simply by coordinating the phase relationship of three independent single-phase inverter controllers, as is often done for other three-phase inverter schemes.

C. CONTROLLER WITH BUCK CHOPPER

This model incorporates a discrete representation of the buck chopper output filter. The equations which govern the filter response can be obtained by applying

Kirchoff's voltage law and Kirchoff's current law to the circuit of Figure (2-1). The equations which describe the ideal operation are:

$$\frac{di_L}{dt} = \frac{d \cdot E - v_C}{L} \tag{4-1}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \tag{4-2}$$

with d defined as the duty cycle, a value between zero and one. The actual circuit operation involves the main switch being operated as open or shut with the duty cycle describing the ratio of shut time to total time. Equations (4-1) and (4-2) were placed in the ACSL code in state-space normal form and integration statements were formulated which allow for the continuous integration of the state variables, v_C and i_L. The power of the ACSL environment is shown by the ability to toggle between the appropriate differential equations which describe the system.

The first set of differential equations is encountered when the main switch for the buck chopper is closed. These equations will include the input voltage, E, and will cause power to be transferred into the main circuit from the source. The diode is simulated as being reverse biased. When the condition is met for the main switch to open, as described in the controller section, the proper differential equations are selected to allow for the diode to be 'on' and the source voltage to no longer provide power to the main circuit. These actions are handled by the PROCEDURAL sections of the code in Appendix A. These sections also allow for the condition in which the current through the inductor becomes discontinuous by setting the inductor current to zero rather than

allowing it to become negative, which is physically impossible. The resistor, capacitor, and inductor values for the buck chopper model were set to 15 Ω, 2000 μF, and 1.35 mH, respectively.

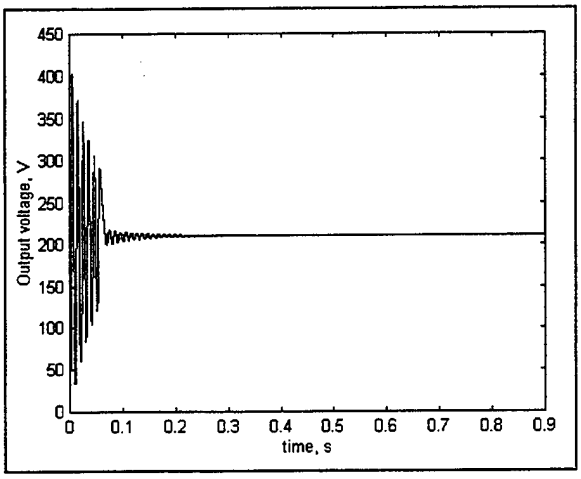

Figure 4-6, Simulated open loop startup response

Figure (4-6) illustrates the expected response of the buck chopper with One-Cycle Control for a constant source voltage and reference voltage. The transient at the beginning of the plot is due to the startup of the circuit with the initial capacitor voltage equal to zero and is seen as the charging of the output filter capacitor and ringing of the LC filter with a small damping resistance. Recall that any disturbance which causes a change in the output voltage will result in an oscillation of the output filter for the open loop case. The stable steady-state output of the circuit is achieved within 0.25 seconds.

1. Open-Loop Source Voltage Step Change

The source voltage step change response of the controller showed that the duty cycle was adjusted within one cycle, but how does the overall circuit respond in an open-

loop configuration? The first source voltage variation simulated was a step change from 300 V to 350 V at 0.3 seconds and back to 300 V at 0.6 seconds. The ACSL model was simulated with the response to this step change shown in Figure (4-7).

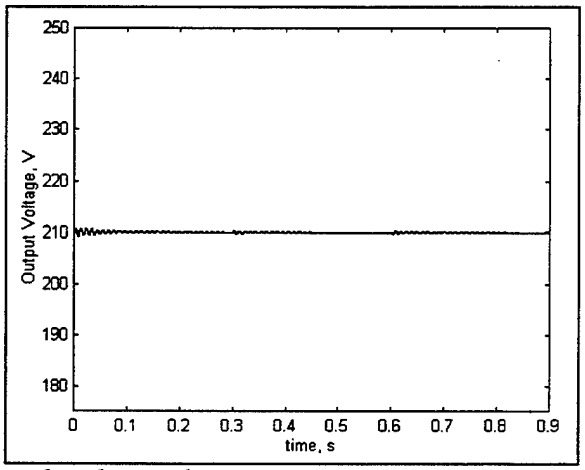

Figure 4-7, Simulated open loop response to a source voltage step change

The input voltage transients were not completely eliminated by the controller. This result was not predicted by the One-Cycle Control theory. The reason for this phenomenon is that the power signal being delivered into the buck chopper is essentially a rectangular pulse train at the switching frequency. When the amplitude of the pulse train is changed appreciably, the output filter of the buck chopper will be excited and a damped oscillation will result. Note that the magnitude of the oscillation is very small compared to the output voltage. To help clarify that this oscillation was not due to the ACSL model or integration algorithm, a separate circuit modeling package, PSPICE, was utilized.

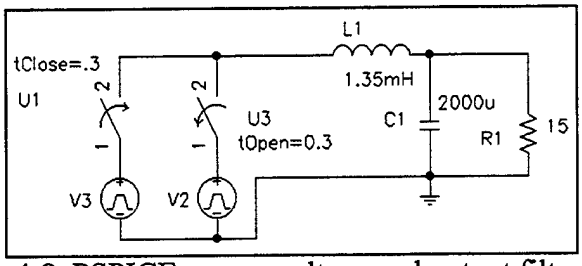

Figure 4-8, PSPICE source voltage and output filter model

The circuit shown in Figure (4-8) represents the buck chopper output filter and the rectangular pulse train from the source as delivered under One-Cycle Control. At 0.3 seconds, the switches operate to remove the first pulse train source and connect the second pulse train source to the output filter. The first pulse train source is comprised of a series of rectangular pulses 300 V in amplitude with an on time of 35 μs and a period of 50 μs. The second pulse train source is comprised of a series of rectangular pulses 350 V in amplitude with an on time of 30 μs and a period of 50 μs. These values correspond to the exact sets of pulses that would be delivered if the duty cycle was fixed at 0.7 and a source voltage step change from 300 V to 350 V was injected.

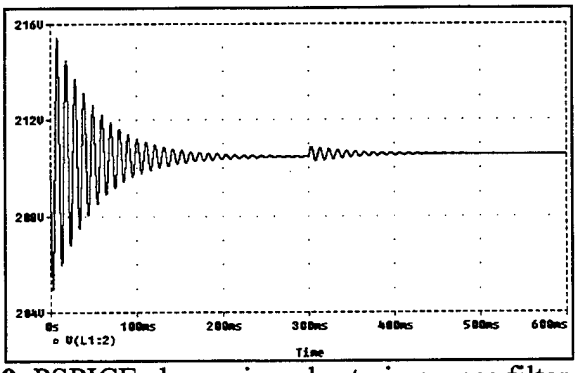

Figure 4-9, PSPICE change in pulse train causes filter excitation

The PSPICE model was run to 0.6 seconds with the results shown in Figure (4-9). Clearly the excitation of the output filter results from a change in the nature of the pulses being input.

For completeness, the ACSL model was run with stopping points at 0.3 seconds and 0.6 seconds, but the source voltage value was not changed. Under this condition, no oscillation was seen. Also, the PSPICE model was run with the two voltage sources identically defined. The switches were allowed to operate in order to change from one source to the other. No oscillations were present in this simulation either. These results show that the simulation packages were not the source of the oscillations.

2. Open-Loop Source Voltage Sinusoidal Variation

Now that the limitation of a source voltage step change has been revealed, the result of a sinusoidal variation in the source voltage would be quite interesting to see. The ACSL model was run with a sinusoidally varying source voltage injected at 0.3 seconds. The input voltage was 300 V_{DC} with an additional component of 30 V_{AC} at a frequency of 60 Hz superimposed upon the DC voltage. The results of this run are shown in Figure (4-10). The One-cycle controller was able to adequately reject this power source periodic perturbation, making the method useful for systems in which the input filtering is crucial. Note that the ripple voltage is approximately 1.0 V and is at the same frequency as the source perturbation. It is also important to note that the corner frequency of the low pass output filter of the buck chopper is above 60 Hz, which may contribute to the oscillation being allowed to propagate through the circuit.

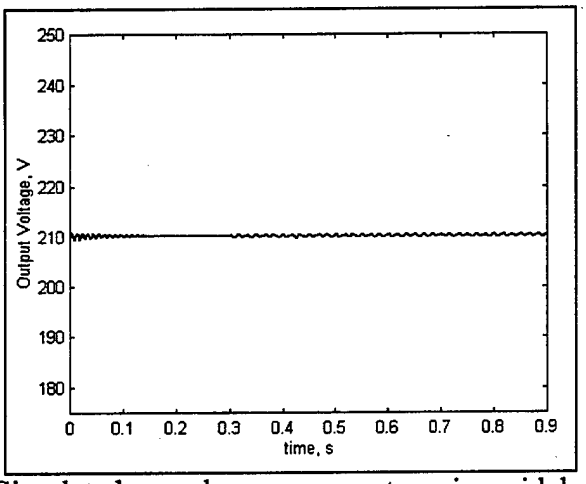

Figure 4-10, Simulated open-loop response to a sinusoidal source voltage

3. Open-Loop Reference Voltage Step Change

The next area explored was the response of the open-loop controller to a change in the reference voltage. Figure (4-11) illustrates the response of the model to a step change in the reference voltage from 0.7 V to 0.8 V at 0.3 seconds and back to 0.7 V at 0.6 seconds.

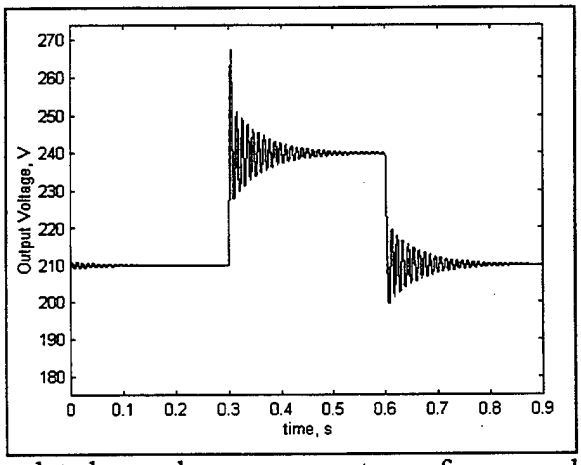

Figure 4-11, Simulated open-loop response to a reference voltage step change

The output voltage achieves a new steady-state value after a transient period which is due to the output filter capacitor of the buck chopper being charged to its new steady-state voltage. It is becoming evident that the controller will require a feedback loop in order to minimize the transients on startup, reference voltage changes, and source voltage variations.

4. Open-Loop Load Step Change

The final type of variation explored within the One-Cycle Control scheme is a load step change. Recall, that the inherent load stability for the buck chopper is defined by the size of the output filter. The smaller the filter components, the higher the resonant frequency induced by a load variation. The output voltage will typically resonate until the load resistance dampens the oscillation sufficiently. The ACSL model was run again with a step change in the output resistance from 15 Ω to 100 Ω at 0.3 seconds and back to 15 Ω at 0.6 seconds. The output voltage of the power circuit with the controller is shown in Figure (4-12).

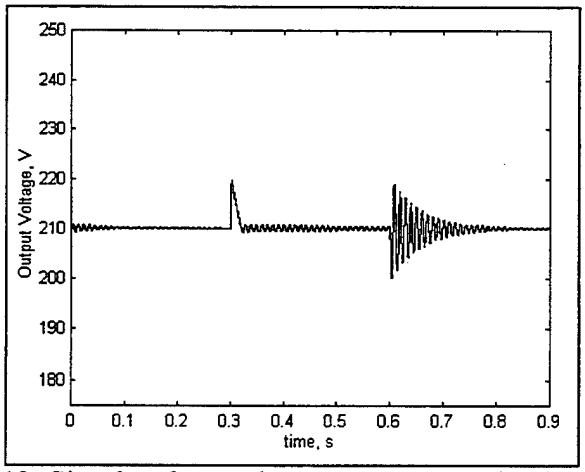

Figure 4-12, Simulated open-loop response to a load step change

The effect of the load change is to cause a resonance which is unacceptable for the control of the power circuit. The solution to the problems encountered is to introduce a feedback loop to the basic controller.

D. CONTROLLER WITH FEEDBACK

The feedback method employed was a simple current feedback loop. The current into the load will remain constant if the load does not change. If the load resistance decreases, the current into the load will increase. The average current into the inductor does not change without feedback applied since the controller has not felt any effect of the load change. By comparing the currents into the load and inductor, a signal which represents the error between the two may be generated and applied to the basic reference voltage of the controller to compensate for the load change.

The One-Cycle controller must make up for this current differential in a short period of time in order to achieve acceptable performance. The gains associated with the current feedback signals are found by describing the differential equations for the buck chopper with the feedback values entered where appropriate. Assuming that all values are scaled to those used within the power section of the circuit, the duty cycle can be described by:

$$d = \frac{V_{ref} + k_1 \frac{v_C}{R} - k_2 i_L}{v_{int,max}} \qquad (4\text{-}3)$$

where V_{ref} is the desired output voltage, k_1 is the load current gain, k_2 is the inductor current gain, and $v_{int,max}$ is the maximum value that the integrator will reach in a given period if not reset until the end of the period. The value of $v_{int,max}$ is defined in such a way that it will always equal the instantaneous, scaled value of the source voltage. Substituting Equation (4-3) into Equation (4-2) and equating the input voltage to the maximum integration voltage results in:

$$\frac{di_L}{dt} = \frac{-k_2}{L} i_L + \left(\frac{k_1 - R}{LR}\right) v_C + \frac{v_{ref}}{L}. \tag{4-4}$$

The state space normal form for the system becomes:

$$\rho \begin{vmatrix} v_C \\ i_L \end{vmatrix} = \begin{vmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{k_1 - R}{LR} & \frac{-k_2}{L} \end{vmatrix} \begin{vmatrix} v_C \\ i_L \end{vmatrix} + \begin{vmatrix} 0 \\ \frac{1}{L} \end{vmatrix} \left| V_{ref} \right| \tag{4-5}$$

where ρ represents the time derivative function. Manipulating the system matrix from Equation (4-5), the characteristic equation of the system is derived as:

$$s^2 + \left(\frac{k_2}{L} + \frac{1}{RC}\right) s + \left(\frac{k_2 - k_1}{LRC} + \frac{1}{LC}\right) = 0. \tag{4-6}$$

In a feedback system such as the one described, there is no closed-form solution available with which to choose the appropriate gain values. The method employed was to use the MATLAB functions 'eig', 'bode', and 'step' with the specified state matrices for the system and observe the results for various gain values. The MATLAB code is included in Appendix B. The gains selected were 3.0 for both k_1 and k_2. The resultant poles for these gains are -178.3 and -2077.3 radians/sec.

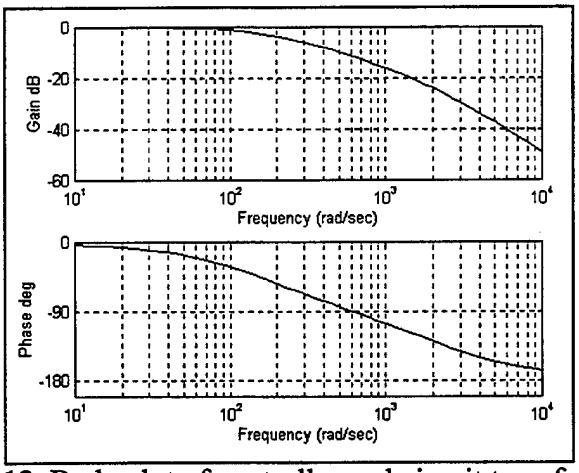

Figure 4-13, Bode plot of controller and circuit transfer function

The Bode plot of Figure (4-13) shows that the phase margin is acceptable and that the gain is sufficiently attenuated at a frequency well below the switching frequency of 20 kHz, thus avoiding positive feedback.

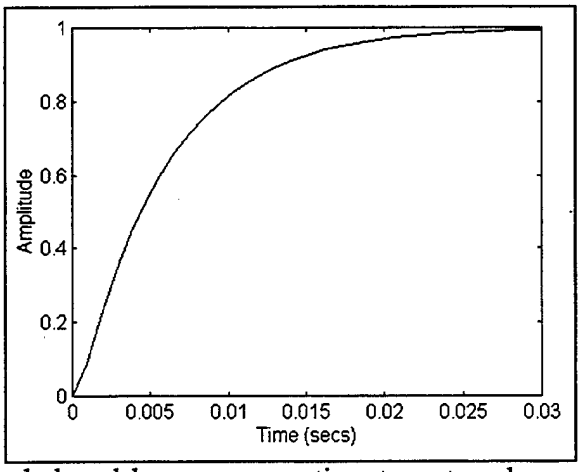

Figure 4-14, Predicted closed-loop response time to a step change in reference voltage

Figure (4-14) shows that the settling time for a unity step change in reference voltage is sufficiently small and that there is no overshoot.

There will be a steady-state error in the output voltage with the feedback loop active since the inductor current term is not averaged. The equation placed in the ACSL code is:

$$duty = V_{ref} + k_1 \cdot I_{Load} - k_2 \cdot I_L \tag{4-7}$$

where 'duty' is the value compared to the integrator voltage for the main switch 'reset' and the constant V_{ref} is the scaled ordered output voltage. Since the 'reset' action is accomplished at the maximum inductor current, the difference between the maximum inductor current and the average inductor current will cause a steady-state error when the gains are matched. Also, any event which causes a change in the maximum inductor current will cause the steady-state error to change.

1. Implementing Feedback

The feedback loop was entered into the ACSL model by placing the two feedback terms and their associated gains, properly scaled, into the expression for the duty cycle. Recall that this value is compared with the integration value in order to determine the state of the main switch. The gain values were scaled to the level of the control system by dividing the raw gains found previously by 300. The scaled gain values used were 0.01 for both k1 and k2 and are able to be modified during a run of the model, if desired. The startup simulation was repeated with the results shown in Figure (4-15). The feedback obviously enhances the control during startup of the circuit. There is no noticeable overshoot and the settling time is on the order of 0.04 seconds. This

of the closed-loop controller when presented with a large voltage transient. In practice, the input current would be limited through the use of a ramp function in the ordered duty cycle.

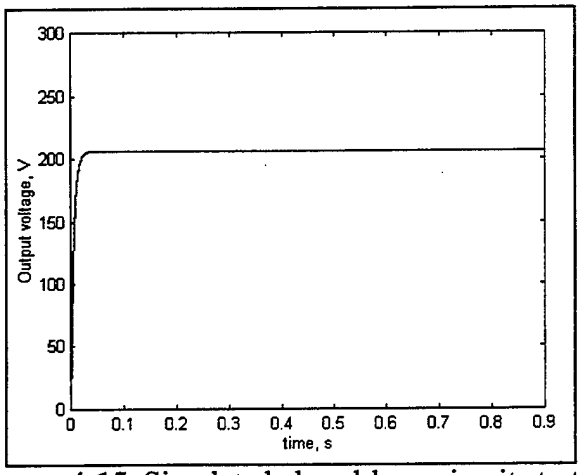

Figure 4-15, Simulated closed-loop circuit startup

2. Closed-Loop Source Voltage Step Change

The ACSL model with feedback was run with the same source voltage step change as that for the open-loop model in order to see if the controller will now reject power source perturbations with the feedback loop active. The result of this simulation is shown in Figure (4-16). One can easily see that the controller is now able to better reject the source perturbation due to the addition of the feedback loop. Note that a steady-state error of approximately 3.0 V with the 300 V input and 5.0 V with the 350 V input is introduced through the use of feedback. Additional work, such as filtering the inductor current signal, might be done to lessen or eliminate this effect.

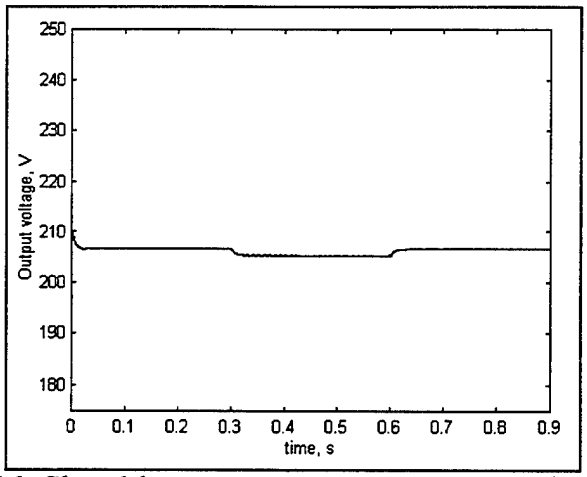

Figure 4-16, Closed-loop response to a source voltage step change

3. Closed-Loop Sinusoidal Source Variation

Once again, the feedback loop model is tested in order to verify that the feedback does not detract from the basic features of the One-Cycle controller. The closed-loop model was simulated with the same sinusoidal source voltage as used in the open-loop case. The results of this simulation are shown in Figure (4-17).

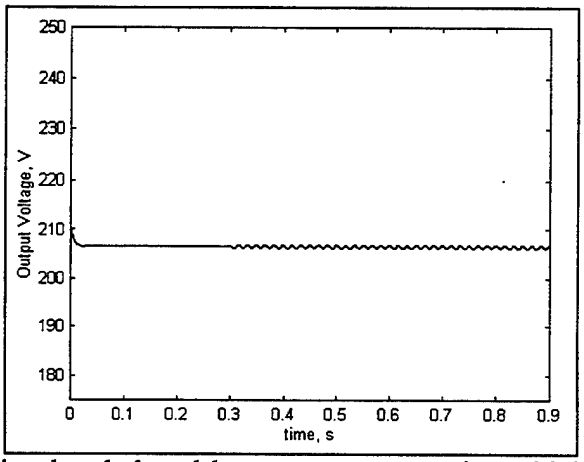

Figure 4-17, Simulated closed-loop response to a sinusoidal source voltage

Again, the closed-loop controller did not cause any adverse effects, allowing for the conclusion that the feedback loop does not cause an unexpected effect on the basic controller. The ripple on the output is not eliminated by the use of feedback.

4. Closed-Loop Reference Voltage Step Change

The effect of the step change in reference voltage with feedback added to the controller should be a much smaller voltage overshoot and faster settling time for the expected transient. The simulation performed was similar to that for the open-loop model with the results illustrated in Figure (4-18).

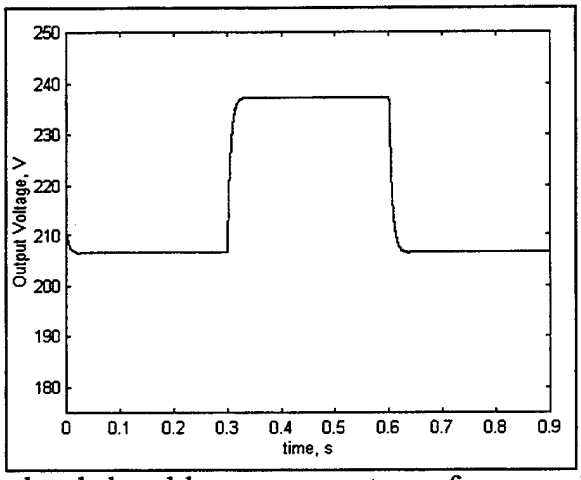

Figure 4-18, Simulated closed-loop response to a reference voltage step change

The feedback loop clearly enhanced the performance of the controller by making the voltage overshoot and settling time for the reference voltage change very small.

5. Closed-Loop Load Step Change

The final test of the feedback loop is in the load response characteristics. The simulation performed was similar to that for the open-loop controller with the results shown in Figure (4-19). The load response is seen to be quite adequate for the system. The transient voltages are approximately 2.0 V and the settling times are on the order of 0.03 seconds. The gains are adjustable to achieve a different response time or overshoot; however, the gains selected give excellent results for the controller. The feedback loop has performed as required, providing enhancement of the controller's inherent source perturbation rejection and acceptable load variation response.

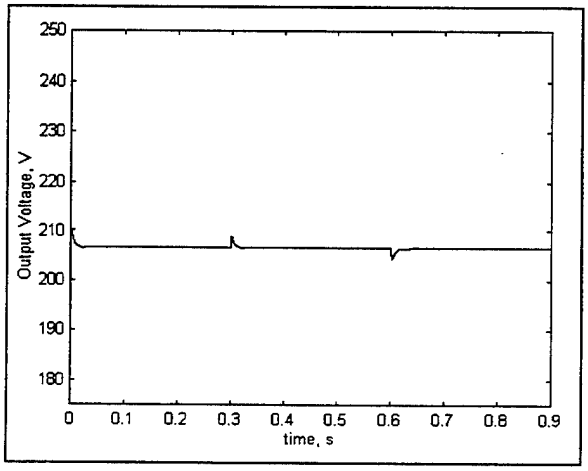

Figure 4-19, Simulated closed-loop response to a load step change

The simulations revealed many important concepts for this control scheme. A direct application via a prototype controller is presented in the next chapter to support these findings.

V. PROTOTYPE CONTROLLER

A. CIRCUIT DESIGN

The prototype circuit design employed several CMOS family devices capable of operating at supply voltages of +15 V and -15 V in order to provide a common power supply and logic level for the entire circuit. This was an important design consideration since the input voltage isolator selected for use will only operate from a +15 V supply. The circuit is analog and should allow for the fastest response times possible. The circuit block diagram depicted in Figure (5-1) illustrates the major subsections of the controller.

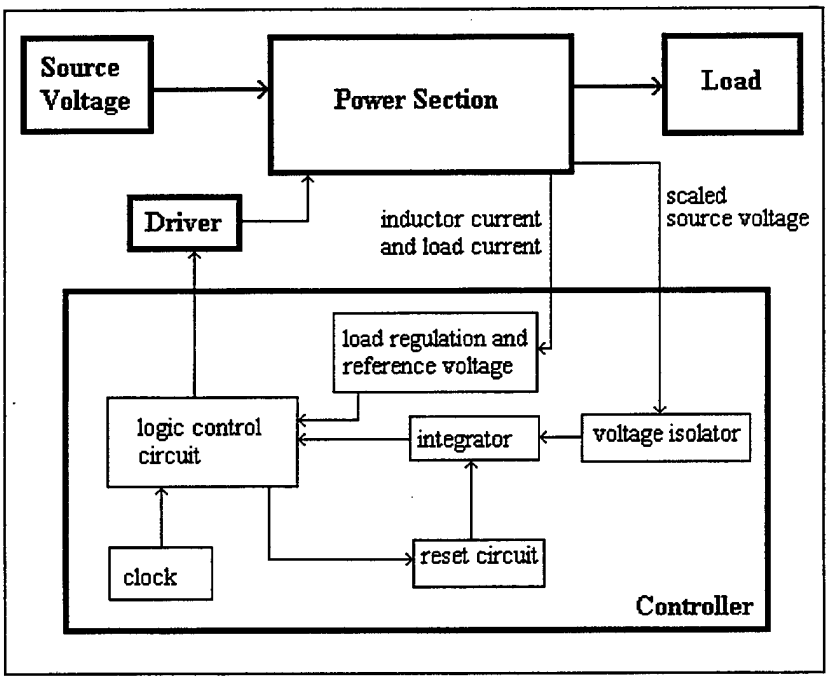

Figure 5-1, Controller block diagram

The interaction of the major controller subsections is straightforward. A clock signal causes the logic control circuit to 'set'. This condition of the logic control circuit 'enables' the integrator, via the reset circuit, and sends a signal to the driver to turn on the IGBT. The scaled source voltage is coupled into the integrator through the voltage isolator. When the integration voltage signal equals the load regulation and reference voltage signal, the logic control circuit is 'reset'. During this state of the logic control circuit, the driver receives a signal ordering the IGBT to turn off and the reset circuit receives a signal causing the integrator capacitor to be discharged, 'disabling' the integrator. The controller and power sections remain in this state until a new clock pulse begins the next cycle of the controller. The inductor current and load current signals are utilized as feedback in the controller.

1. Power Supplies

The power supplies required for the controller are +15 V and -15 V DC. The method for generation of the floating ground reference supplies was similar to that for the unregulated driver circuit power supplies. The floating ground was required due to the nature of the laboratory power supplied to the buck chopper and test equipment. Figure (5-2) shows the schematic diagram for the power supplies. All integrated circuit supply pins on the controller breadboard have 0.1 μF bypass capacitors to ground for transient response and elimination of high-frequency noise on the power busses. A 120/24 V_{AC}, 60 Hz center-tap transformer and full wave bridge rectifier with 2200 μF capacitors for ripple smoothing yields unregulated +21 V and -21V.

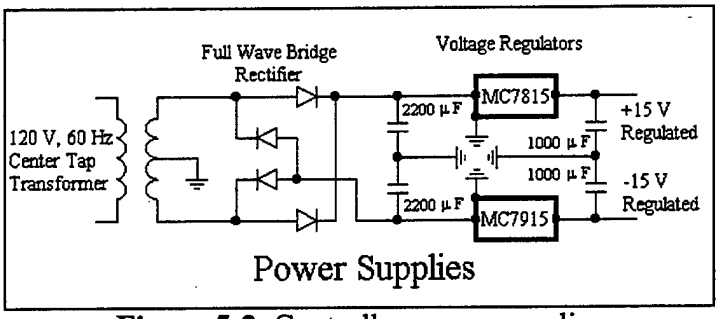

Figure 5-2, Controller power supplies

The unregulated voltage is fed to a set of voltage regulators, producing ±15 V. These three-terminal positive and negative voltage regulators, the MC7815 and MC7915, respectively can handle in excess of 1 Amp output current with proper heat sinks. Output bypassing of these regulators was accomplished using 1000 µF capacitors to ground.

2. Clock Circuit

The clock circuit, Figure (5-3), for the controller breadboard is constructed from a single LM555CN timer chip.

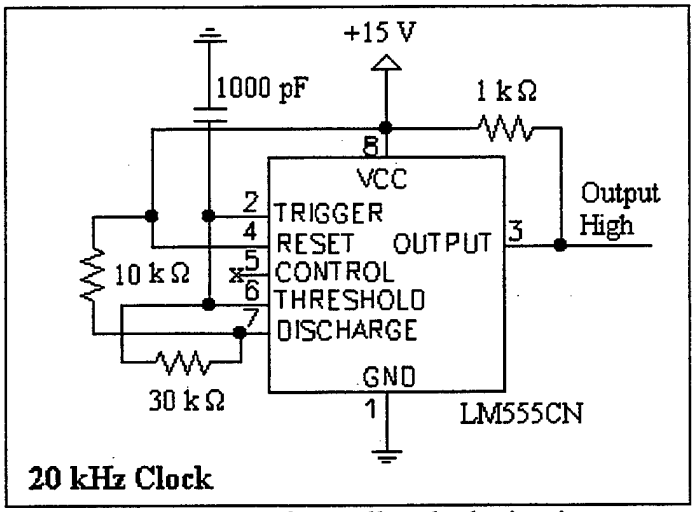

Figure 5-3, Controller clock circuit

The equation which governs the period of the clock circuit is:

$$T = 0.693(R_a + 2R_b)C \tag{5-1}$$

where the resistor R_a is connected between pins 4 and 7, the reset and discharge terminals of the chip, and the resistor R_b is connected between pins 2 and 7, the trigger and discharge of the chip. The capacitor, C, is connected between pin 2, the trigger, and ground. The values for R_a, R_b, and C were found to be 10 kΩ, 30 kΩ, and 1000 pF, respectively, yielding a theoretical period of 48.51 μsec. The period as tested was 48.6 μsec, corresponding to a frequency of 20.6 kHz.

A load resistance, R_L, is required for proper circuit operation and was arbitrarily chosen as 1 kΩ. Since only the rising edge of the clock pulse will be used, the duty cycle of the waveform is not important.

3. Integrator

Perhaps the most important component of the One-Cycle controller is the integrator. It must provide linear integration over the entire range of scaled input voltages. To construct the integrator, an LM741CN operational amplifier chip and 0.01 μF capacitor were utilized as shown in Figure (5-4). The basic operation of the circuit constructed dictates that the output voltage will be proportional to the integral of the input voltage. The positive terminal of the operational amplifier was tied to ground via a 1.0 kΩ resistor, and the negative terminal was tied to the input signal via another 1.0 kΩ resistor. Since the period of the controller is very short and the integrator is reset to zero every cycle, the DC bias currents of the 741 did not cause significant error.

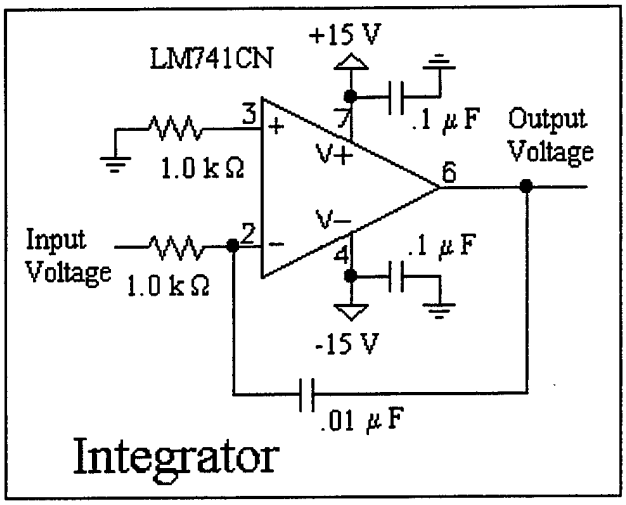

Figure 5-4, Controller integrator

The operation of the integrator was found to be linear over the range of scaled input voltages from 0 to 5 V. The use of a "chopper stabilized" operational amplifier was considered for this application in order to further reduce the effects of DC offset voltage and input current bias errors, but was not necessary.

4. Reset Circuit

The other crucial component of the One-Cycle controller is the integrator reset circuit shown in Figure (5-5). In the ideal case, the integrator is fully reset, in zero time, to the same reference value at the beginning of each integration cycle. To achieve this, the reset switch would be required to have a zero impedance and no rise or fall times. Since we cannot obtain such a switch, some error will be introduced into the controller. The reset switch used for this application is a CD4066BE quad bilateral semiconductor switch. It has a typical on-state resistance of 80 Ω .

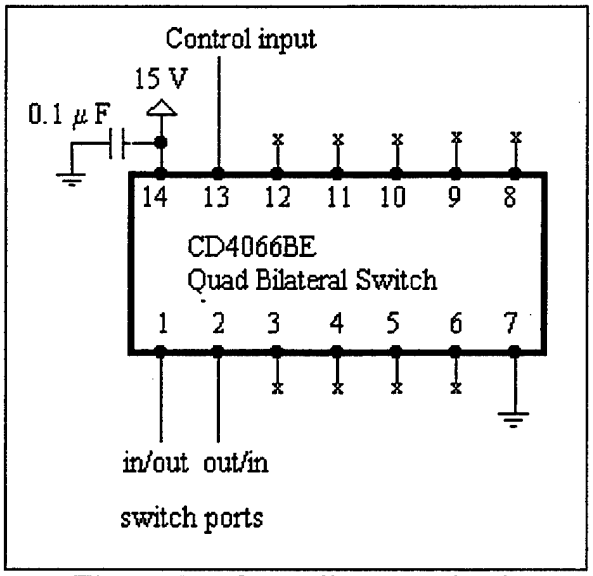

Figure 5-5, Controller reset circuit

The switch will assume the on-state whenever the input to the control terminal is high. The switch ports were connected to either side of the integrator capacitor in order to facilitate the reset action. The typical reset time for the integrator was found to be 4 μsec, and was independent of the number of reset switches paralleled within the chip.

5. Voltage Sensing Circuit

An AD215 voltage isolation amplifier was utilized for the input electrical connection between the power circuit and the controller. The circuit configuration is shown in Figure (5-6). A voltage divider comprised of 130 Ω and 43 kΩ resistors was used to scale the input voltage to a level suitable for the AD215 and the AD215 provides the necessary electrical isolation for the control circuit. The voltage range for the AD215 is ±10 V. Note that a few watts will be dissipated in the 43 kΩ resistor so it must be rated accordingly.

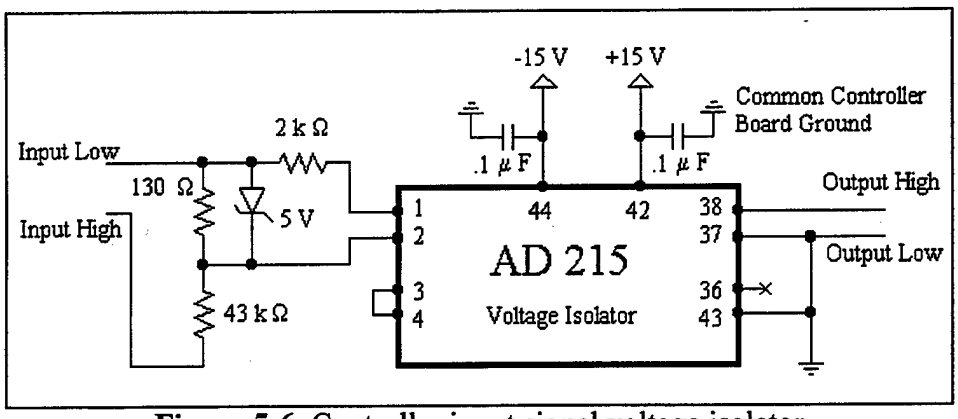

Figure 5-6, Controller input signal voltage isolator

The 5 V zener diode limits the maximum voltage input to the AD215 in the event that the voltage divider network fails. In addition, a 2 kΩ resistor on the input of the AD215 protects the device from excessive current should the zener fail during a voltage transient. The AD215 was configured for non-inverting operation, hence pins 3 and 4 were tied together. The integrator requires a negative input voltage in order to generate the positive output voltage for use in the comparator. In order to achieve an inverted input to the integrator, the inputs to the voltage isolator were inverted. This is much simpler than setting up the voltage isolator circuit in an inverting configuration. Linearity of the circuit was tested satisfactorily over the range of expected frequencies and voltages.

6. Logic Control Circuit

The control circuit includes a flip-flop and two LM311N comparators as shown in Figure (5-7). Comparator # 1 is used to generate the reset signal in order to turn off the IGBT of the buck chopper power section. The signals compared are the reference voltage and the integrator voltage. If the reference voltage on pin 2 is higher than the output of

the integrator on pin 3, the active high 'reset' pin of the 4027 is pulled 'high' through a 5.1 kΩ resistor.

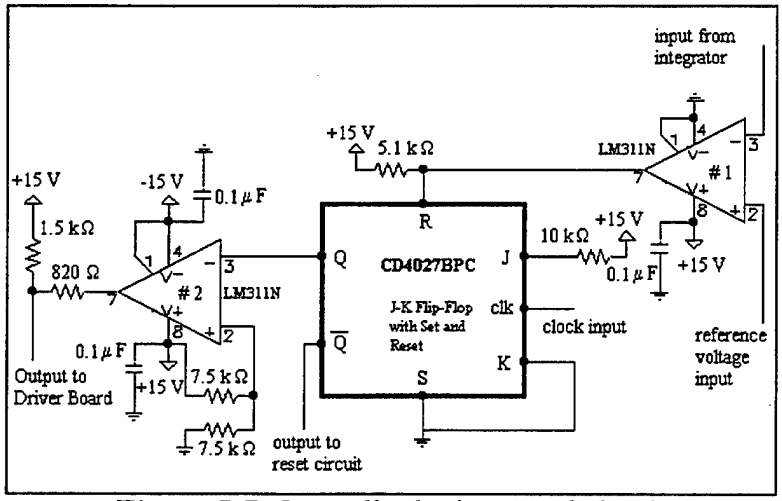

Figure 5-7, Controller logic control circuit

A CD4027BPC dual J-K master/slave flip-flop with set and reset was configured to provide the switching logic. When a rising edge trigger is seen by the flip-flop clock terminal, the device will set, due to the J terminal being tied to +15 V through the 10 kΩ resistor. This state will be maintained until an asynchronous reset signal is seen by the reset pin, when the device will 'reset' to logic '0'. This condition is met in the manner previously described. Note that the flip-flop will not 'set' if the asynchronous reset pin is held at a 'high' state. This feature may be useful to facilitate an unconditional main circuit shutdown. The Q terminal is high whenever the device is set, and low whenever the device is reset.

The other LM311 comparator was chosen as the output stage delivering the pulsed control signal to the buck chopper driver circuit. The resistances on the output of the comparator were selected to ensure that the proper voltage and current levels were present to drive the photodiode inside the TLP 250. Recall that the TLP 250 is an optical isolator driver chip designed exclusively for IGBT transistors. The photodiode within this chip will be activated by comparator # 2 when the flip-flop is 'set' and deactivated when the flip-flop is 'reset'.

7. Load Regulation and Reference Voltage Circuit

The load regulation and reference voltage circuit features three additional LM741CN operational amplifiers as seen in Figure (5-8).

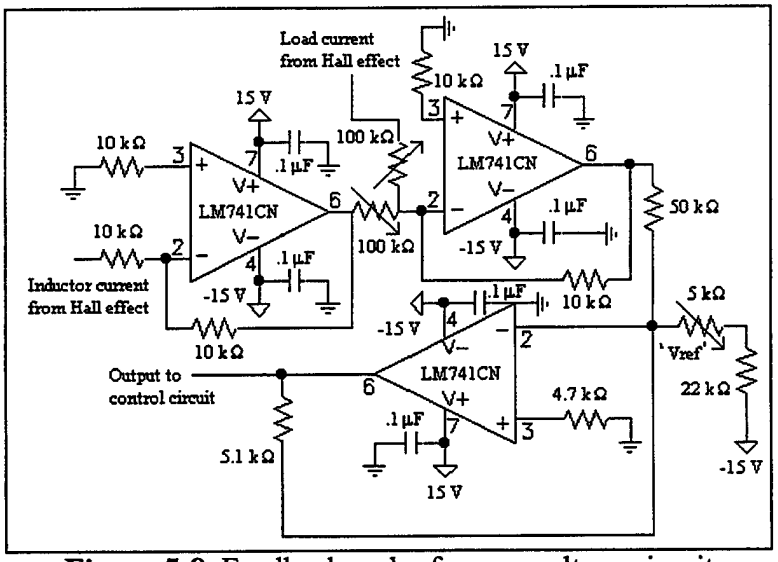

Figure 5-8, Feedback and reference voltage circuit

The op-amp on the left side of the figure is used to generate the negative-valued inductor current signal. It is a unity gain inverting design. The operational amplifier in the upper

right portion of the figure is a 'summing' amplifier which adds the positive load current signal to the negative inductor current signal. The input resistors to this 'summing' amplifier are 10 turn adjustable 100 kΩ potentiometers. This allows trimming of the feedback gains as desired. The current feedback is introduced into the third operational amplifier which also acts as a 'summing' amplifier. The 50 kΩ input resistance and the 5.1 kΩ feedback resistance provide the coupling for the current feedback signal into the basic reference voltage. The 5 kΩ adjustable resistor and the 22 kΩ fixed resistor connected to the -15 V power supply in conjunction with the 5.1 kΩ feedback resistance form the reference voltage section. This voltage is adjustable from 2.75 V to 3.25 V and corresponds to a buck chopper output voltage range of $170\ V \leq V_{out} \leq 200\ V$.

The current signals were sensed using two NNC-20GA Hall effect sensors. The sensors are part of the fixed laboratory equipment and were not integrated into the controller breadboard. The voltage signals generated by these sensors were 0.1 V per Amp of sensed current.

B. CONTROLLER BENCH TESTS

The controller was bench tested to ensure proper operation prior to connection to the power section. Various inputs were used including a sine wave to evaluate the unit's robustness. The first test conducted was a basic controller run with a constant scaled source voltage of approximately 1.1 V and integration reference voltage of 3.25 V as shown in Figure (5-9). The time scale is 20 μs per division and the voltage scales are 1, 2, and 20 V per division for the source, integrator and duty cycle voltages respectively.

The result is a periodic steady state integration wave form and constant duty cycle. The integration voltage is seen to be 'reset' at the same reference voltage for each cycle, and when the integrator resets, it assumes the same voltage level in the 'low' state for each cycle.

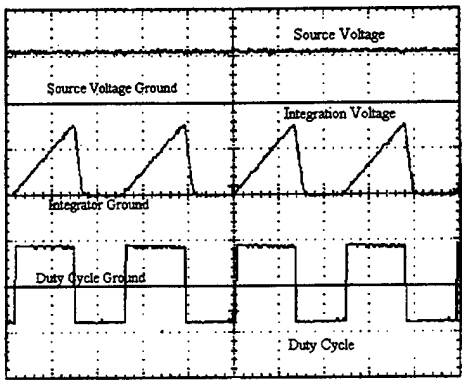

Figure 5-9, Basic Controller Operation

The duty cycle signal varies between approximately +15 V and -15 V, with the ground level as shown. The duty cycle assumes the high state when the cycle begins and is seen to assume the low state when the integrator voltage reaches the reference level. The integrator waveform and duty cycle pulses are synchronized.

1. Source Voltage Step Change Response

Recall that the step change in source voltage for the One-Cycle Control technique should yield a dynamic change in the duty cycle to the new steady-state duty cycle within one period. For the source voltage step change, the scaled source voltage injected into the control circuit was from a function generator operating at a frequency of 3.6 kHz, in the square-wave mode, with a maximum value of 1.45 V and a minimum value of 0.8 V.

Figure (5-10) shows the scaled source voltage, the integrator output, and the resultant duty cycle. The time scale is 50 μs per division and the voltage scales are 1, 2, and 20 V per division for the source, integrator and duty cycle voltages respectively.

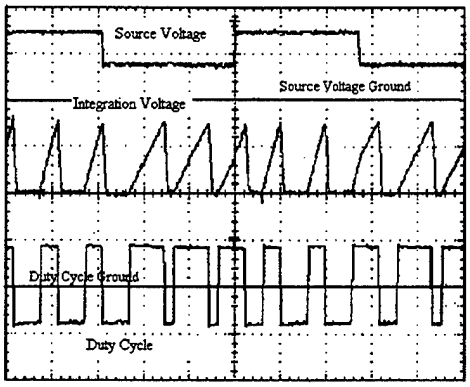

Figure 5-10, Controller response to a source step change

Clearly the duty cycle is greater when a smaller source voltage is present and is dynamically adjusted within one cycle as the source voltage shifts to a higher value. The results illustrated in Figure (5-10) closely match the theory and simulation results for a step change in the source voltage. The basic theory of One-Cycle Control is supported by these results. Closer inspection of the plot shows that the duty cycle associated with the source voltage at the higher level will yield the same average output voltage each cycle as the duty cycle associated with the source voltage at the lower level. Linearity of the control system is shown by this result.

2. Source Voltage Sinusoidal Variation Response

The source voltage was then changed to a sinusoidal input with a steady-state DC value. The amplitude of the maximum and minimum values of the input were 1.45 V and

0.8 V respectively, and the frequency was 3.6 kHz. The integration voltage and duty cycle are seen to dynamically change with the input voltage on a per cycle basis in Figure (5-11). The time scale is 50 μs per division and the voltage scales are 1, 2, and 20 V per division for the source, integration, and duty cycle voltages, respectively.

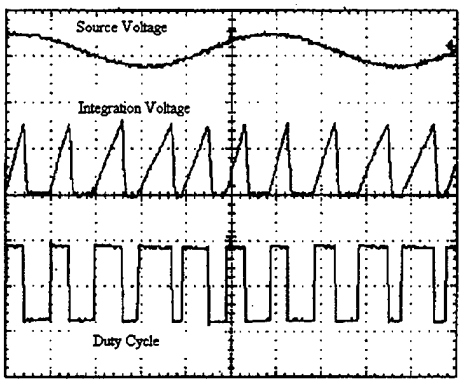

Figure 5-11, Controller response to a sinusoidal source voltage

A larger duty cycle is seen when the sinusoid is at the minimum value and vice versa. The duty cycle variation is in such a manner as to eliminate the source perturbation, thus the effect of the variation in source voltage should be minimized in the output circuit. The results of the sinusoidal variation of the source voltage are similar to those found in the simulations. The frequency of the perturbation, 3.6 kHz in this case, must be significantly below the switching frequency of the converter if adequate rejection of the perturbation is to occur. In this case the higher sinusoidal frequency was chosen merely to demonstrate the ability of the controller to adjust the duty cycle in the proper manner on a scale which is readable.

3. Reference Voltage Step Change Response

With the source voltage held constant, the reference voltage was varied as a square wave with a frequency of 1.2 kHz, and maximum and minimum values of 1.45 and 0.8 V, respectively. Figure (5-12) shows that the response to a step change in the reference voltage occurs in one cycle, with zero steady-state or dynamic error.

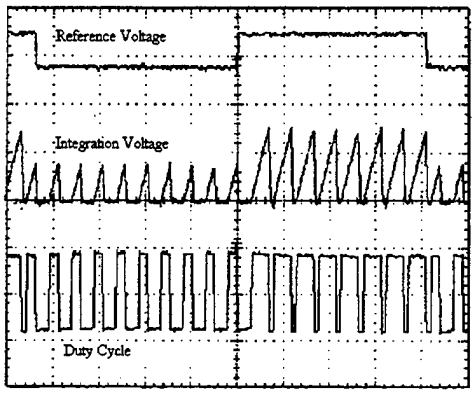

Figure 5-12, Controller response to a reference voltage step change

The time scale is 100 μs per division and the voltage scales are 1, 1, and 20 V per division for the reference, integration, and duty cycle voltages, respectively. Once again, the simulation and prototype test results show the same behavior.

4. Sinusoidal Reference Voltage Response

A 3 kHz sinusoidal reference voltage was injected into the controller with the source voltage held constant and minimum and maximum voltages of 1.45 V and 0.8 V for the reference. The result shown in Figure (5-13) appears very similar to the sine PWM signal discussed earlier. The time scale is 100 μs per division and the voltage scales are 1, 1, and 20 V per division for the reference, integration, and duty cycle

voltages, respectively. The simulation results again accurately predicted the actual controller response. The ability of the One-Cycle controller to generate a signal suitable for use in an AC inverter is thus shown.

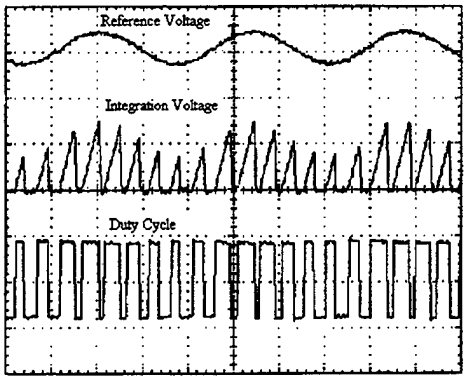

Figure 5-13, Controller response to a sinusoidal reference voltage

C. OPEN-LOOP OPERATION

The One-Cycle controller was connected to the buck chopper in an open-loop configuration for a battery of tests, including a source voltage step change response, a source voltage sinusoidal perturbation response, a reference voltage step change response, and a load step change response. The open-loop configuration was achieved by disconnecting the current feedback from the summing node of the reference voltage operational amplifier. A goal of less than 2 % voltage overshoot was arbitrarily established. The results of these tests follow.

1. Source Voltage Step Change

The source voltage was varied via the use of a 120/120 V, 60 Hz isolation transformer, a 120 V AC variac, and a rectifier to obtain an adjustable floating reference DC voltage source. The source was added to the main power source through the use of a steering diode and high power transistor switch, allowing for a source voltage step change to be generated. The voltage values selected for the step change were 300 V and 350 V, and the frequency of the step changes was 0.1 Hz. The power circuit was connected to a high power load resistance to yield an output current of 5 A, and operated at an output voltage of 185 V for a total output power of 925 W.

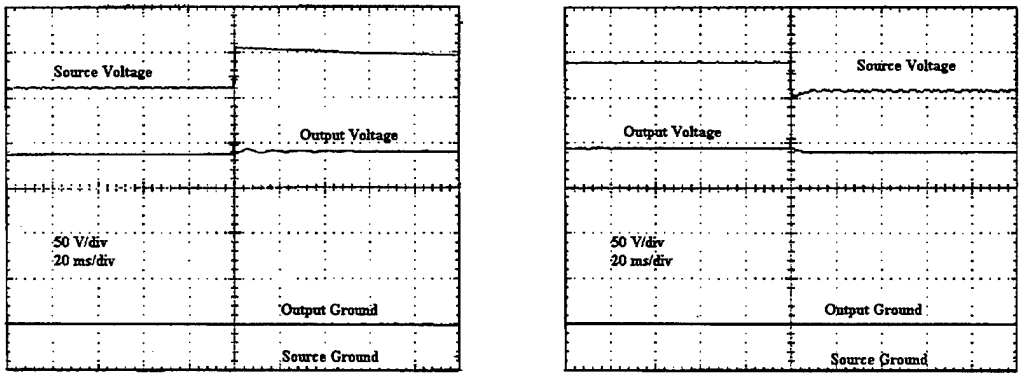

Figure 5-14, Open-loop response to a source voltage step change

The results of the source voltage transients are illustrated in Figure (5-14). The One-Cycle controller was able to eliminate the source voltage transients in an effective manner. The transient for the step change in the source voltage to a higher value, shown on the left, appears to be more limiting. The maximum overshoot is on the order of 2 V and the steady-state difference between the output voltages before and after the transients is also about 2 V. This difference between the output voltages given different input

voltages is due to non-ideal component effects within the power and control circuits. A voltage feedback loop might be incorporated to eliminate the non-ideal component effects, however, the inherent speed of the One-Cycle Control scheme may be jeopardized. Finally, the maximum transient time is on the order of 40 to 60 ms for the output filter, which is acceptably short. The simulation results support the response obtained for the circuit. With these results, a feedback loop would not be necessary.

2. Source Voltage Sinusoidal Variation

The input filter of the power circuit was removed in order to subject the buck chopper to the raw output of a 3-phase, full wave bridge rectifier. This source voltage has the characteristic of a 360 Hz ripple riding on the basic DC voltage as shown in Figure (5-15).

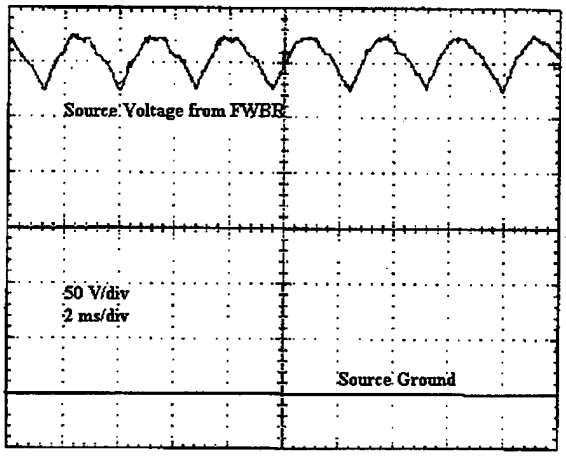

Figure 5-15, Source voltage from an unfiltered 3-phase rectifier

The 'average' voltage of the source was 300 V with the ripple voltage magnitude on the order of 50 V. Figure (5-16) shows how the One-Cycle controller is able to virtually

eliminate the large ripple voltage present on the input of the buck chopper. The output voltage waveform was magnified in order to show that the ripple voltage is on the order of 0.2 V and the frequency of the ripple does not correlate with the input voltage ripple frequency. The output ripple frequency is approximately 125 Hz, which is close to the resonant frequency of the output filter. The simulation results predicted a slightly larger magnitude of 1.0 V for the ripple voltage as well as a slightly lower frequency of 60 Hz; however, the circuit results still match the simulation fairly well. A possible cause of the discrepancy between the ripple voltage frequencies is that damping dynamics were not modeled in the simulations. In any event, the output voltage waveform is quite acceptable without a feedback loop added.

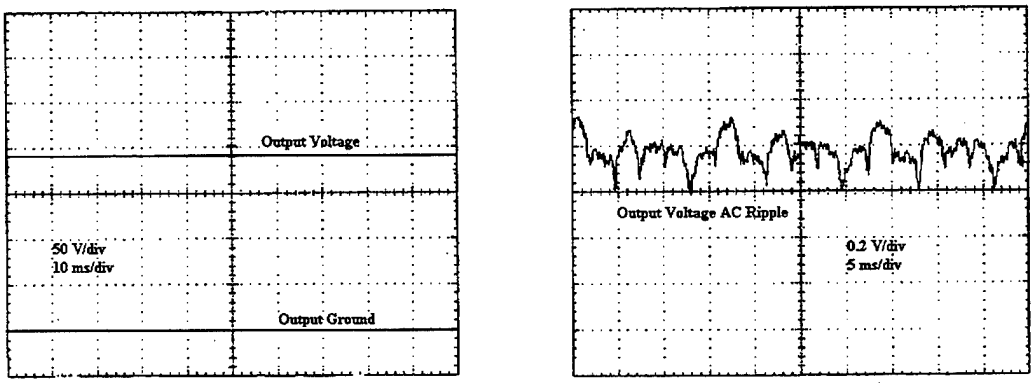

Figure 5-16, Open-loop response to a "sinusoidal" source voltage

3. Reference Voltage Step Change

Recall that the simulation for the reference voltage step change showed a fairly large overshoot for the open-loop case. For the circuit test, the reference voltage was varied from 0.8 V to 1.45 V at a frequency of 0.1 Hz. Figure (5-17) illustrates that the

output voltage achieves a new steady-state value only after a transient which is associated with the output filter capacitor being charged. The step change from the lower reference voltage to the higher voltage is shown on the left. The voltage overshoot is on the order of 8 V or 4.3 % and the settling time is on the order of 40 ms. For the step change from a higher reference voltage to a lower reference voltage, shown on the right, the voltage overshoot is on the order of 2 V or 1.1 % with a settling time of about 30 ms. These results are in agreement with the simulations. Since the voltage overshoot exceeds 2 % for the upward step change, a feedback loop can now be justified.

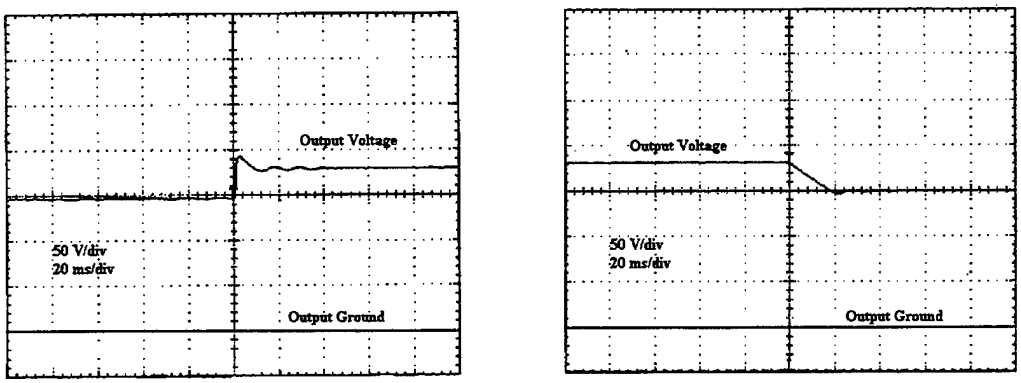

Figure 5-17, Open loop response to a reference voltage step change

4. Load Variation

Simulations showed that the load step change would induce oscillations in the output voltage which exceed the desired specification of 2 %. In order to evaluate the overall open-loop response to load step changes, the load bank was manipulated in such a way as to yield a stepped output resistance of approximately 14 Ω and 100 Ω at a frequency of 0.1 Hz. This corresponds to an approximate output power step change from

2500 W to 300 W. Figure (5-18) shows that the step change from a larger load resistance to a smaller load resistance, shown on the left, yields an oscillation with a voltage overshoot of about 8 V or 4.3 % and a settling time of 40 ms.

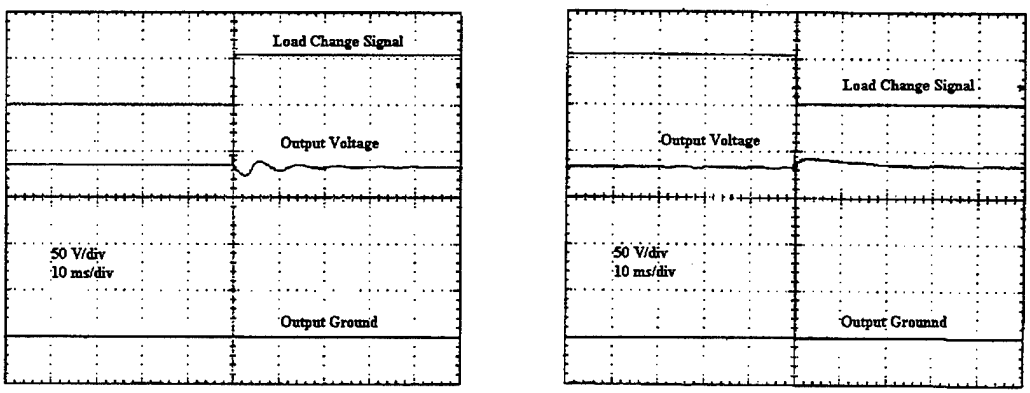

Figure 5-18, Open-loop response to a load step change

For the step change from a smaller load resistance to a larger load resistance, the voltage overshoot is about 5 V or 2.7 % and the settling time is 30 ms. Both results exceed the 2 % overshoot criteria. These results are in agreement with the simulations and allow the conclusion that a feedback network is required for this control scheme.

D. OPERATION WITH CURRENT FEEDBACK

The feedback loop was connected as discussed previously and the exact same battery of tests was run on the power circuit. The feedback gains k1 and k2 were identically set to 0.0255 which was experimentally determined to give good results. A discussion of the gain selection is presented at the end of this chapter. The results of these tests follow.

1. Source Voltage Step Change

The closed-loop source voltage step change response is shown in Figure (5-19). For the step change in either direction, there is no noticeable overshoot and the time to achieve the steady-state output voltage is on the order of 10 ms. The difference in the output voltages, recall, is the result of non-ideal circuit components and feedback error and is on the order of 2 V with feedback employed. This result is well within the desired 2 % limit. The results also correspond well with the simulations.

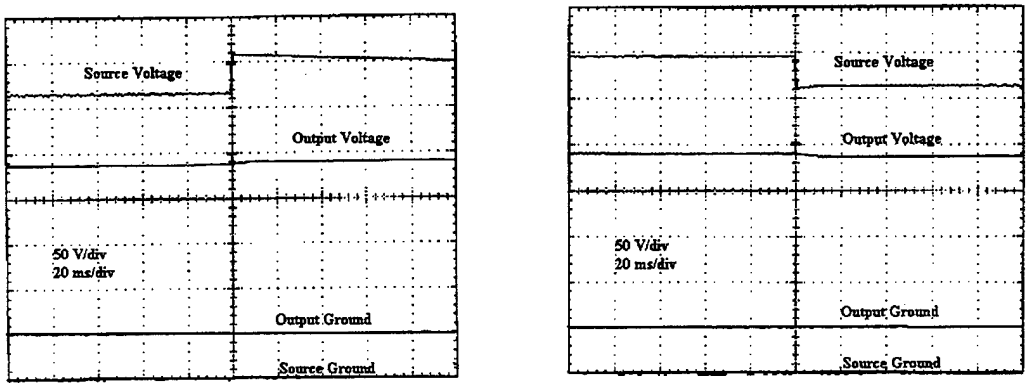

Figure 5-19, Closed-loop response to a source voltage step change

2. Sinusoidal Source Voltage Variation

Figure (5-20) shows the closed-loop response to the source voltage sinusoidal variation. Recall that the source voltage is the raw output of the bridge rectifier as seen in Figure (5-15). The source perturbation was rejected and the feedback loop did not cause any adverse affects on the One-Cycle controller. Again, the output voltage was magnified to show the ripple. Note that the ripple voltage is still about 0.2 V with the feedback loop active. The result of this run is also in agreement with the simulations.

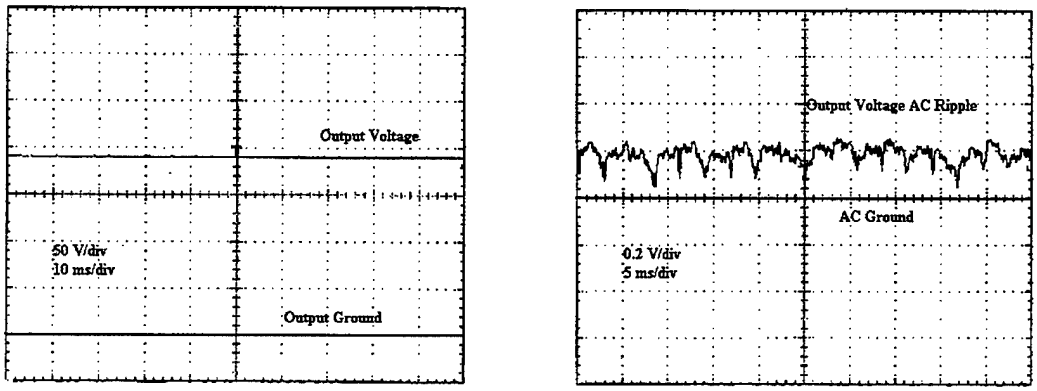

Figure 5-20, Closed-loop response to a "sinusoidal" source voltage

3. Reference Voltage Step Change

The closed-loop reference voltage step change results are illustrated in Figure (5-21). Note that there is no overshoot in either case and that the maximum settling time, in this case for the step down in reference voltage, is 20 ms. The feedback loop successfully removed the undesired overshoot. Similar results were shown through the simulations.

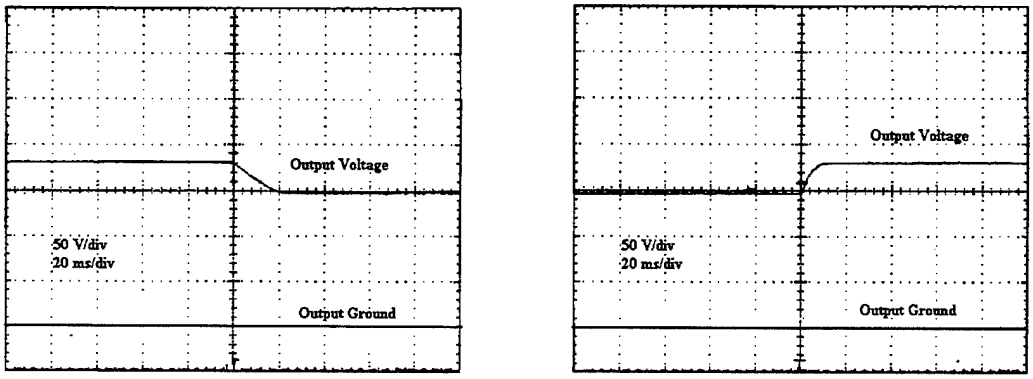

Figure 5-21, Closed-loop response to a reference voltage step change

4. Load Regulation

The final closed-loop circuit test performed was the load step changes. Figure (5-22) shows that there is no overshoot and that the settling time is identical for both the higher and lower resistance steps. Once again, the feedback loop was able to eliminate the undesired overshoot. The simulations yielded a similar result for this test. The steady-state voltage error in this case is on the order of 2 V, which is acceptable.

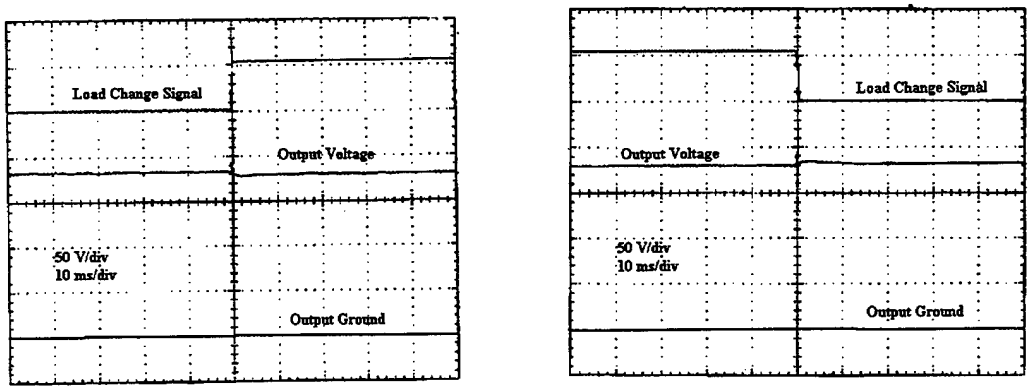

Figure 5-22, Closed-loop response to a load step change

A discussion of the selection of the values for the feedback gains is in order. Table (5-1) shows the maximum overshoot and settling time for the step change in load for various values of the feedback gain, where the gains k1 and k2 are set equal.

Feedback Gain	Maximum Overshoot (V)	Settling Time (msec)
[illegible]	1 (0.5 %)	[illegible]
[illegible]	2 (1.1 %)	[illegible]
[illegible]	3 (1.6 %)	[illegible]
[illegible]	5 (2.7 %)	[illegible]
[illegible]	5 (2.7 %)	[illegible]
[illegible]	7 (3.8 %)	[illegible]
[illegible]	8 (4.3 %)	[illegible]
open loop	10 (5.4 %)	[illegible]

Table 5-1, Current feedback gain response

The gain value required to yield a voltage overshoot less than 2 % was determined to be about 0.015. The actual gain employed was 0.025 to ensure that any voltage transients would be well within specification. The resultant poles are at -65.7 and -5634.3 rad/sec, thus the system is stable. The scaled gain value used in the simulations would have resulted in an actual gain on the prototype board of 0.05. In fact, the gain may be set higher than that attempted without encountering instability, but the results found for the gain selected are quite good and gains above 0.038 did not improve the performance of the controller noticeably.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY OF RESULTS

The ability of the One-Cycle Control technique to properly control the buck chopper has been established, but how does the controller measure up to the criteria for the research listed in the introduction? The first requirement was that there is no steady-state nor dynamic error between the control signal and the control variable. Recall that the control variable was not the output voltage of the buck chopper, but rather the diode voltage. As seen with the controller operating without the power section attached, this claim is true. However, the pulsed nature of a step change applied to the power section and thus its filter did result in the creation of an oscillation. This does not present a particularly difficult problem to solve, and a current feedback loop adequately eliminated output filter oscillations.

The second requirement was that the technique would yield robust performance. This is a difficult area to judge. The controller was only tested under laboratory conditions; however, the range of source voltages applied to the controller was widely varied as well as the application of the raw output of a three-phase rectifier. The power levels tested were large enough such that meaningful results for shipboard power conversion could be uncovered. During the performance of all testing phases, there was no indication of controller instability. Also, the buck chopper was constructed as a hard-switched converter, thus producing large amounts of electromagnetic interference during

operation. During all of these 'adverse' conditions, the controller performed admirably, so the conclusion that the control scheme is robust must be in order.

Next was the ability of the controller to perform power source perturbation rejection. Recall that the perturbation selected was quite dynamic. The source voltage was set at 300 V with a 360 Hz, 50 V ripple riding on top. This type of power source would probably be very difficult to use given a conventional feedback controller, but the One-Cycle controller was easily able to eliminate this undesirable perturbation.

In regards to fast dynamic response to changes in the control signal, the controller was able to respond to the change within one period. The controller with power section achieved the steady state within 40 ms of a transient while operating open loop and 20 ms while operating closed loop. The limiting element in reference voltage dynamic response does not lie within the controller, but rather the power circuit being controlled due to the filter response.

The ability to generate a sine PWM signal was demonstrated, thus the control technique can be applied to more than one type of switch control; however, general switch control application was not fully shown in this research. Also, automatic switching error correction, discussed in Chapter III, Section D, was not achieved due to the controller sensing location. Several attempts to build the better integration and reset circuits described in References [1] and [2] were not met with success due to the limitations of devices available in the laboratory. Automatic switching error correction was not specified as a design goal; however, a proposal to overcome device limitations and availability is presented in the next section.

B. FUTURE RESEARCH AREAS

The power of the One-Cycle Control technique might be fully realized through further research into better integrator and reset switch design. Other areas which would be of benefit to the Navy would include the extension of One-Cycle Control to inverter controllers, and possible implementation of this technique into the PEBB research.

1. AC Power Generation

The Navy is currently constructing several prototype inverters for use in a test bed to gain a better understanding of the interactions between the components of DC ZEDS. Control of these inverters involves the generation of signals such as sine PWM in order to achieve proper operation. A simple test of this control scheme within the inverter realm might involve using the prototype controller presented to generate a single phase AC power source to validate the theory. Further extension of this research into the Digital Signal Processing (DSP) arena might prove useful. The SSIMs are intended to be controlled by a master computer and a generic DSP controller which is programmable for the application desired.

2. Digital Signal Processing Application

The processing power of modern DSP chips is making the implementation of more complex control algorithms possible. The speed at which the DSP controller can switch a power converter is also increasing. The advantage of One-Cycle Control in the DSP controller area is the power, simplicity, and generality of the method. This control technique is based on the integral equations describing the controlled variable, thus the

control is more closely coupled to the system, as compared to standard feedback control. The benefit that the One-Cycle Control technique might gain from DSP implementation is the possibility of a 'perfect' integrator and reset switch. This would allow full utilization of the automatic switching error correction feature of this method. With error correction enabled, the only feedback loop necessary for a buck chopper would be for load regulation, which this research has investigated. The simulation code in this research might prove valuable in the formulation of One-Cycle Control algorithms for DSP controller use.

3. PEBB General Controller

As the PEBB becomes more defined and the specific control techniques are researched, the power, simplicity, and generality of the One-Cycle Control technique may prove useful in this endeavor. This technique is available now and can be implemented in computer and DSP controllers for the PEBB.

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9. Mitchell and Gauthier Associates, *Advanced Continuous Simulation Language Reference Manual*, 1993.

10. Franklin, G. F., Powell, J. D., Emami-Naeini, A., *Feedback Control of Dynamic Systems*, Addison-Wesley Publishing Company, Reading, MA, 1994.

APPENDIX A. ACSL SIMULATION CODE

```
! "ACSL model for buck chopper and One-cycle controller"


PROGRAM

INITIAL
        "-----this section is not sorted,  it typically contains"
        "    constants and the determination of initial values"
        "    for use in the DERIVATIVE section"

        MAXTERVAL maxt = 10.0e-8    !"maximum integration step size"
        MINTERVAL mint = 10.0e-8    !"min time step: for var step size"

        CINTERVAL cint = 50.0e-6    !"data communication interval"
        ALGORITHM ialg = 5          !"integration algorithm"
                                    !"4--R.K. 2nd, 5--R.K. 4th"
        NSTEPS   nstp = 1
        CONSTANT tstop = 0.5        !"stop point for integration"
        CONSTANT Rout1 = 15.0       !"output load resistance"

        CONSTANT Vref = .7          !"basic reference voltage"

        CONSTANT vinac = 0.0          !"source sinusoidal perturbation"
        CONSTANT vindc = 300.0        !"basic source voltage"
        CONSTANT pertfreq = 377.0     !"perturbation frequency"

        "-------Buck parameters"
        CONSTANT Lbuck1 = 1.35e-3               !"inductance L"
        CONSTANT Cbuck1 = 2000.0e-6             !"capacitance C"
        CONSTANT Vdidrop1 = 0.0                         !"diode drop"
        CONSTANT Vswdrop1 = 0.0                         !"switch drop"
        CONSTANT rampperiod1 = 50.0e-6                  !"ramp period"

        "----assign the initial inductor current and cap volt"
        CONSTANT iLic1 = 14
        CONSTANT Vcic1 = 210

        "----assign the controller feedback gains"
        CONSTANT k1 = 0.0
        CONSTANT k2 = 0.0

        "----define and initialize the switch conduction status"
        LOGICAL SW11
        SW11 = .true.         !"T s1 conducts, F s1 blocks"

        "----define and initialize variable which keeps track of"
        "   whether the converter is in cont or discont mode"
        LOGICAL contmode1
        contmode1 = .true.       !"T contin, F discontin"
```

```
END ! "of initial"

DYNAMIC
        "----this section is executed each cint seconds"

        "----statement required to stop simulation at tstop seconds"
        TERMT (t .GE. tstop)
        reframp1=0.0                !"resets the integrator each cycle"

 DERIVATIVE
        "----this section is executed each maxt seconds and is sorted"

        "----determine conduction status of SW1"
        PROCEDURAL(SW11,isw1=reframp1,duty,iL1)
                "----charge inductor when duty GT reframp"
                IF (duty .GT. reframp1) THEN
                        SW11 = .true.
                        isw1 = iL1
                ELSE
                        SW11 = .false.
                        isw1 = 0.0
                ENDIF
        END                     !"of procedural"

        "----Given conduction status of SW11, and whether"
        "   continuous or not, determine derivative of iL1"
        PROCEDURAL(piL1=SW11,contmode1,vbuckin,Vc1,Vdidrop1, &
                  Vswdrop1,Lbuck1)

                "----if SW11 gated, assume can conduct pos. current"
                IF (SW11) THEN
                        contmode1 = .true.
                        piL1 = (vbuckin-Vswdrop1-Vc1)/Lbuck1
                ELSE
                        "----if iL1 GT zero the diode conducts"
                        IF (contmode1) THEN
                                piL1 = (-Vdidrop1-Vc1)/Lbuck1
                        ELSE
                                piL1 = 0.0    !"discontin mode"
                        ENDIF
                ENDIF
        END             !"of procedural"

        "----Evaluate the derivative of the capacitor voltage"
                pVc1 = (iL1 - Vc1/Rout1)/Cbuck1

        "----Integrate the state variables"
                iL1 = INTEG(piL1, iLic1)
                Vc1 = INTEG(pVc1, Vcic1)

        "----Establish the reference One-cycle waveform"
        "   used for determining when SW1 is gated on"
        vbuckin = vindc + vinac*sin(pertfreq*t)
```

```
            Vsensed=vbuckin/300.0
            reframp1 = INTEG(Vsensed/rampperiod1, 0.0)

        "----Establish FEEDBACK to alter basic duty cycle"
            duty = Vref+(k1*Vc1/Rout1)-(k2*iL1)

        "----Schedule discontinuous mode when iL tries go neg"
        SCHEDULE DCM1 .XN. iL1


END ! "of derivative"

        "----establish transition to discontinuous mode"
        DISCRETE DCM1
            contmode1 = .false.
        END     !"of dcm1"


END ! "of dynamic"

END ! "of program"
```

```
! "This file is used to study the controller and power circuit"

s strplt = .t.                    ! "one variable per x-axis"
s calplt = .f.

s devplt = 1                      ! "6 for X-windows"
                                  ! "5 for postscript"

s ppoplt = .f.                    ! "true rotates plot 90 deg"

s xinspl = 6                      ! "x-axis plot units"

s weditg = .f.                    ! "false suppresses data write"
                                  ! "each time SCHEDULE occurs"

s nrwitg = .f.                    ! "true enables accumulation of data"
                                  ! "after a CONTIN"

prepare t,Vc1

proced study1             ! "Input voltage step change response"
 s tstop = 0.3
 s nrwitg = .f.
 s vindc = 300.0
 start
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = 0.6
 s vindc = 350.0
 s nrwitg = .t.
 contin
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = 0.9
 s vindc = 300.0
 contin
 plot vc1 /lo=0.0 /hi=300.0
end

proced study2                     ! "Load step change response"
 s tstop = 0.3
 s nrwitg = .f.
 start
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = 0.6
 s nrwitg = .t.
 s Rout1 = 100.0
 contin
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = 0.9
 s Rout1 = 15.0
 contin
 plot vc1 /lo=0.0 /hi=300.0
end
```

```
proced study3                    ! "Reference voltage step change response"
 s tstop = 0.3
 s nrwitg = .f.
 start
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = 0.6
 s Vref = 0.8
 s nrwitg = .t.
 contin
 plot vc1 /lo=0.0 /hi=300.0
 s tstop = .9
 s Vref = 0.7
 contin
 plot vc1 /lo=0.0 /hi=300.0
end

proced study4                    ! "Source voltage sinusoidal response"
 s tstop = 0.3
 s nrwitg = .f.
 start
 plot vc1 /lo=0.0 /hi=300.0
 s nrwitg = .t.
 s tstop = 0.9
 s vinac = 30.0
 contin
 plot vc1 /lo=0.0 /hi=300.0
 s vinac = 0.0
end
```

```
! "ACSL model for buck chopper and One-cycle controller"
! "modified for modeling the controller only"

PROGRAM

INITIAL
        "-----this section is not sorted,  it typically contains"
        "    constants and the determination of initial values"
        "    for use in the DERIVATIVE section"

        MAXTERVAL maxt = 10.0e-8   !"maximum integration step size"
        MINTERVAL mint = 10.0e-8    !"min time step: for var step size"

        CINTERVAL cint = 1.0e-7    !"data communication interval"
        ALGORITHM ialg = 5         !"integration algorithm"
                                   !"4--R.K. 2nd, 5--R.K. 4th"
        NSTEPS    nstp = 1
        CONSTANT tstop = 250e-6    !"stop point for integration"
        CONSTANT Rout1 = 15.0      !"output load resistance"

        CONSTANT Vref = .7        !"basic reference voltage"

        CONSTANT vinac = 0.0           !"source sinusoidal perturbation"
        CONSTANT vindc = 300.0         !"basic source voltage"
        CONSTANT dutyac = 0.0          !"reference sinusoidal signal"
        CONSTANT pertfreq = 22619.4    !"frequency for perturbations"

        "-------Buck parameters"
        CONSTANT Lbuck1 = 1.35e-3              !"inductance L"
        CONSTANT Cbuck1 = 2000.0e-6            !"capacitance C"
        CONSTANT Vdidrop1 = 0.0                        !"diode drop"
        CONSTANT Vswdrop1 = 0.0                        !"switch drop"
        CONSTANT rampperiod1 = 50.0e-6                 !"ramp period"

        "----assign the initial inductor current and cap volt"
        CONSTANT iLic1 = 13.5
        CONSTANT Vcic1 = 208.1

        "----assign the controller feedback gains"
        CONSTANT k1 = 0.0
        CONSTANT k2 = 0.0

        "----define and initialize the switch conduction status"
        LOGICAL SW11
        SW11 = .true.         !"T s1 conducts, F s1 blocks"

        "----define and initialize variable which keeps track of"
        "   whether the converter is in cont or discont mode"
        LOGICAL contmode1
        contmode1 = .true.       !"T contin, F discontin"


END  ! "of initial"
```

```
DYNAMIC
        "----this section is executed each cint seconds"

        "----statement required to stop simulation at tstop seconds"
        TERMT (t .GE. tstop)

 DERIVATIVE
        "----this section is executed each maxt seconds and is sorted"

        "----determine conduction status of SW1"
        PROCEDURAL(SW11,isw1,dutyout=reframp1,duty,iL1)
                "----charge inductor when duty GT reframp"
                IF (duty .GT. reframp1) THEN
                        SW11 = .true.
                        isw1 = iL1
                        dutyout=1.0        !"used for plotting"
                ELSE
                        SW11 = .false.
                        isw1 = 0.0
                        dutyout=0.0
                ENDIF
        END                     !"of procedural"

        "----Given conduction status of SW11, and whether"
        "   continuous or not, determine derivative of iL1"
        PROCEDURAL(piL1=SW11,contmode1,vbuckin,Vc1,Vdidrop1, &
                  Vswdrop1,Lbuck1)

                "----if SW11 gated, assume can conduct pos. current"
                IF (SW11) THEN
                        contmode1 = .true.
                        piL1 = (vbuckin-Vswdrop1-Vc1)/Lbuck1
                ELSE
                        "----if iL1 GT zero the diode conducts"
                        IF (contmode1) THEN
                                piL1 = (-Vdidrop1-Vc1)/Lbuck1
                        ELSE
                                piL1 = 0.0    !"discontin mode"
                        ENDIF
                ENDIF
        END             !"of procedural"

        "----Evaluate the derivative of the capacitor voltage"
                pVc1 = (iL1 - Vc1/Rout1)/Cbuck1

        "----Integrate the state variables"
                iL1 = INTEG(piL1, iLic1)
                Vc1 = INTEG(pVc1, Vcic1)

        "----Establish the reference One-cycle waveform"
        "   used for determining when SW1 is gated on"
        vbuckin = vindc + vinac*sin(pertfreq*t)
```

```
            Vsensed=vbuckin/300.0
            reframp1 = INTEG(Vsensed/rampperiod1, 0.0)

        "----Establish FEEDBACK to alter basic duty cycle"
            duty = Vref+(k1*Vc1/Rout1)-(k2*iL1) &
               + dutyac*sin(pertfreq*t)   !"for sinusoidal vref"

        "----Schedule discontinuous mode when iL tries go neg"
        SCHEDULE DCM1 .XN. iL1


END ! "of derivative"



        DISCRETE ramp1
            INTERVAL tsamp1 = 50.0e-6
            reframp1 = 0.0
        END    ! "of discrete"

        "----establish transition to discontinuous mode"
        DISCRETE DCM1
            contmode1 = .false.
        END       !"of dcm1"


END ! "of dynamic"

END ! "of program"
```

```
! "This file is used to study the controller without"
! "regard to the power circuit."

s strplt = .t.                    ! "one variable per x-axis"
s calplt = .f.

s devplt = 1                      ! "6 for X-windows"
                                  ! "5 for postscript"

s ppoplt = .f.                    ! "true rotates plot 90 deg"

s xinspl = 6                      ! "x-axis plot units"

s weditg = .f.                    ! "false suppresses data write"
                                  ! "each time SCHEDULE occurs"

s nrwitg = .f.                    ! "true enables accumulation of data"
                                  ! "after a CONTIN"

prepare t,duty,reframp1,vsensed,dutyout

proced study1              ! "Input voltage step change response"
  s tstop = 125e-6
  s nrwitg = .f.
  s vindc = 300.0
  start
  plot reframp1,vsensed,dutyout
  s tstop = 250e-6
  s vindc = 400.0
  s nrwitg = .t.
  contin
  plot reframp1,vsensed,dutyout /xlo=0.0 /xhi=250e-6
  s vindc = 300.0
end

proced study2                     ! "Input voltage sinusoidal response"
  s tstop = 500e-6
  s vinac = 50.0
  s nrwitg = .f.
  start
  plot reframp1,vsensed,dutyout /xlo=0.0 /xhi=500e-6
  s vinac = 0.0
end

proced study3                     ! "Reference voltage sinusoidal response"
  s tstop = 500e-6
  s vref = .5
  s dutyac = .45
  s nrwitg = .f.
  start
  plot duty,dutyout /xlo=0.0 /xhi=500e-6
  s dutyac = 0.0
  s vref = .7
  end
```

```
proced study4                          ! "Reference voltage step change response"
  s tstop = 125e-6
  s nrwitg = .f.
  start
  plot duty,dutyout
  s tstop = 250e-6
  s vref = .8
  s nrwitg = .t.
  contin
  plot duty,dutyout /xlo=0.0 /xhi=250e-6
  s vref = .7
end
```

APPENDIX B. MATLAB FEEDBACK GAIN CODE

```
% m-file to assist in finding gain values

R=15;
E=300;
L=1.35e-3;
C=2000e-6;
k1=3.0;
k2=3.0;

A=[-1/(R*C),1/C;-1/L+(k1)/(L*R),-(k2)/(L)];
B=[0;1/L];
C1=[1,0];
D=[0];

lamda=eig(A)

x=[1,((k2/L)+1/(R*C)),...
  ((k2)/(R*C*L)+1/(C*L)-(k1)/(L*C*R))];

y=roots(x)

figure(1)
bode(A,B,C1,D);

figure(2)
step(A,B,C1,D)
```

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